PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2002-175039
(43)Date of publication of application : 21.06.2002

(51)Int.Cl. G09G 3/20
G02F 1/133
G09G 3/30
G09G 3/36

(21)Application number : 2001-006940
(22)Date of filing : 15.01.2001

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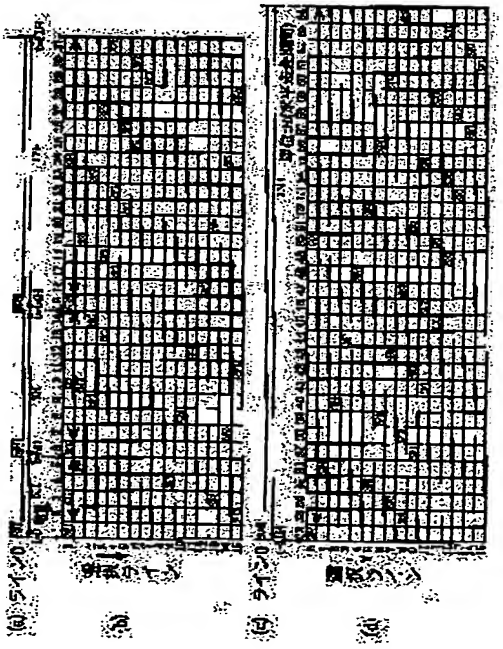
(30)Priority

Priority number	Priority date	Priority country
2000005503	14.01.2000	JP
2000097305	31.03.2000	JP
2000300063	29.09.2000	JP

(54) ACTIVE MATRIX DISPLAY AND DRIVE METHOD THEREFOR

(57)Abstract:
PROBLEM TO BE SOLVED: To provide an active matrix display and a drive method therefor, with which multi-gradation display is carried out by sub-frames, and moreover, flickers are prevented from occurring while shortening a frame period.
SOLUTION: In the drive method for the active matrix display for which one frame is composed of a plurality of sub-frames consisting of a write period and a hold period, and the gradation display is performed by the accumulative effect of the hold periods, during the holding period of each sub-frame related to a prescribed single scanning line, the remaining scanning lines except for the prescribed single scanning line are scanned at random, according to a prescribed order so that writing will not be carried out in the same sub-frame related to the same scanning line, and as an entire single frame period, the gradation display driving is performed with the write and hold periods of each plural sub-frames, substantially secured in each scanning line.



LEGAL STATUS
[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the display which performs a multi-tone display in time in detail with the combination of the voltage level of binary [in a ******** subframe period with weight], or a multiple value, and its drive approach about the display of an active matrix especially liquid crystal, the display that used organic electroluminescence (electroluminescence), and its drive approach.
[0002]
[Description of the Prior Art] Fewer power consumption is demanded of the display used for the small pocket device by cell drive. Liquid crystal and organic electroluminescence (electroluminescence) are known as a representation rank of the display device which fills such a demand. It is common to control the brightness of a pixel and to perform a gradation display according to the electrical potential difference or current of an analog, in the indicating equipment of an active matrix using these display devices and the indicating equipment which uses the thin film transistor (TFT) of three terminals as a switching element typically. For example, when impressing the electrical potential difference of an analog in the case of liquid crystal, by passing the current of an analog, in the case of organic electroluminescence, the brightness of a display device is changed, and it is indicating by gradation.
[0003] The configuration of the conventional active-matrix liquid crystal panel is shown in drawing 10 , and the gradation method of presentation is explained. 101 is the liquid crystal panel of an active matrix, and consists of signal lines S1-Sn, the scanning lines G1-Gm which intersect perpendicularly with this, and a switching element near [the] the intersection. Si is an example of the thin film transistor (TFT) of a switching element and three common terminals in this case which a certain signal line and Gj have in a certain scanning line, and 102 has near [those] the intersection. 103 shows a liquid crystal device and Counterelectrode Vcom is formed in the side which stands face to face against a transistor 102. 104 is storage capacitance, assisted the capacity component of a liquid crystal device 103, and has prevented degradation of image quality. Common connection of the electrode by the side of the reverse is separately made as Vst in many cases. The intersection 105 by the side of these transistors is equivalent to a pixel electrode.
[0004] If actuation is explained briefly, the scanning line Gj will serve as quantity potential once at an one-frame period, it will be made to flow through a transistor 102, and the pixel electrode 105 103, i.e., liquid crystal capacity, and storage capacitance 104 will be charged to Counterelectrode Vcom to the potential of the signal line Si at this time. The scanning line Gj serves as low voltage after that, a transistor 102 is un-flowing, and this charged potential is maintained during the one-frame period. Moreover, although it is common to carry out an alternating current drive as for liquid crystal, the pulse-like wave which reversed Counterelectrode Vcom and the common electrode Vst of storage capacitance synchronizing with the signal line Si is added, and, generally decreasing the amplitude of a signal line Si is also performed. 106 is a shift register by the side of a signal, and a latch, by the clock signal CKH and start signal STH which are inputted from the outside, carries out the sequential sampling of the video signal, and carries out serial-parallel conversion. In drawing 10 , the example of a digital video signal is shown, a two or more bits video signal is changed into an analog signal by the D/A conversion circuit 107, and current amplification is carried out with an

operational amplifier 108, and it is added to signal lines S1-Sn. A scan side consists of the shift register 109 and output buffer 110 which are scanned from a top to the bottom one by one with the clock signal CKV added from the exterior, and a start signal STV, and drives the scanning lines G1-Gm with pulse shape.

[0005] The wave form chart of each part is shown in drawing 11 . HD shows a Horizontal Synchronizing signal, and the period is the horizontal scanning period H, and is equal to the period of above-mentioned STH and above-mentioned CKV. These phases are changed a little with a panel property etc. An input signal is a digital video signal and data change with the period of CKH. FF1, FF2, and FF3 show the sampling pulse of a signal side shift register. For example, in the case of gradation [4 bits and / 16], if data are expressed in hexadecimals, "F" is sampled and latched to "7" and FF3 by "0" and FF2 at FF1. If D/A conversion of this is carried out to the timing of a latch pulse, the pulse height to the opposite potential Vcom will change, and gradation will be expressed now. If opposite reversal is carried out, in case the alternating current drive of liquid crystal will be carried out, it is possible to set about 1/of voltage swings of a signal line to 2, and, generally it is carried out. in addition, overlapping the preceding paragraph gate (although not shown in drawing Gj- 1), forming the storage capacitance 104 of drawing 10 , impressing a pulse voltage from the gate side of the preceding paragraph, and having kept opposite potential constant -- opposite reversal -- the same -- the voltage swing of a signal line -- about -- there is a capacity-coupling drive which can be reduced to one half (JP,3-35218,A). Or effectiveness with the same said of the case of the capacity-coupling drive (Japanese Patent Application No. 11-255228) which impresses a pulse voltage to storage capacitance independently of the gate is acquired, without making storage capacitance 104 overlap the preceding paragraph gate.

[0006] The selection sequence of the scanning line is shown in drawing 12 . An axis of abscissa is time amount and an axis of ordinate is selection Rhine. The minimum width of face of a time-axis is the horizontal scanning period H, and the number of display Rhine is 16. Like drawing 12 , selection sequence is 0->1->2->... It is scanned sequentially like ->15. Therefore, an one-frame period is completed by 16H, and the writing of the following frame starts. In fact, although a perpendicular blanking period is established at a frame period in addition to the Rhine selection time amount, it is omitting in drawing 12 . In addition, the horizontal scanning period H is equal to the period of HD of drawing 11 , and the analog signal is written in the pixel in this time amount. Next, the configuration of the conventional active-matrix organic EL panel is shown in drawing 13 . The case of the liquid crystal panel of drawing 10 and the thing of this function attach the same number. 401 is the organic EL panel of an active matrix, and consists of signal lines S1-Sn, the scanning lines G1-Gm which intersect perpendicularly with this, and a switching element near [the] the intersection. Si is the 1st and 2nd switching elements which a certain signal line and Gj have in a certain scanning line, and 402 and 403 have near [those] the intersection, and shows the thin film transistor (TFT) of three terminals. 404 is auxiliary capacity and carries out the role holding the electrical potential difference of the signal line Si impressed to the gate electrode of the 2nd transistor 403 through the 1st transistor 402. The location of 405 shows a pixel electrode and is connected to the current supply line Vs through the 2nd transistor 403. 406 is an organic EL device, it is formed between the pixel electrode 405 and Counterelectrode Vcom, emits light according to the current which flows between Counterelectrode Vcom and the electrical-potential-difference supply line Vs, and performs a gradation display by the current control. About actuation of a level drive circuit and a vertical-drive circuit, it is the same as that of the case of the liquid crystal of drawing 1 , and scan the scanning line Gj sequentially, it is made to flow through the 1st transistor 402, and the analog voltage outputted to the signal line Si is written in the 2nd gate and auxiliary capacity 404 of a transistor 403.

[0007] As mentioned above, at a conventional active-matrix liquid crystal panel and a conventional organic EL panel, the gradation display has been performed in modulating brightness in analog. Therefore, the D/A conversion circuit was prepared in the level drive circuit, and the electrical potential difference or current of an analog quantity needed to be outputted to the panel. However, it was the factor in which it is necessary to form an operational amplifier in the latter part of a D/A conversion circuit as a current buffer for carrying out the charge and discharge of the signal-line capacity which is a load, and this increases the power consumption of the whole drive circuit. Because, since a static current flows continuously and is continuing the operational amplifier, even

when having not carried out the charge and discharge of the load, and a number equal to the total number of signal lines of operational amplifiers moreover existed, total of the power consumption by the static current of an operational amplifier became large, and this had accounted for the big rate in the power consumption of the whole drive circuit.

[0008] Moreover, in order to control brightness by the gradation display of a active-matrix organic EL panel with the amount of currents which flows to an organic EL device, the display quality of a panel is very sensitive to dispersion in the current-voltage characteristic of a pixel transistor. Therefore, in order to prevent the image quality fall of brightness nonuniformity etc., it is necessary to form transistor characteristics in homogeneity over the whole panel.

[0009] The drive approach that a time amount modulation performs a gradation display in digital one only using a binary fixed electrical potential difference is learned not using analog circuits, such as a D/A converter and an operational amplifier, as one approach of solving these power technical problems and an image quality technical problem. In this application, this shall be called digital gradation means of displaying. In digital gradation means of displaying, dispersion in the transistor characteristics which there is no power loss by the static current of an analog circuit, and are demanded from high definition is not severe, either.

[0010] The configuration of the conventional digital gradation means of displaying is shown by making the case of liquid crystal into an example at drawing 14 . The analog multiplexer 501, i.e., the decoder, and analog switch 502 with which drawing 14 chooses the binary fixed electrical potential differences VH and VL instead of a D/A conversion circuit and an operational amplifier as compared with drawing 10 are arranged. A decoder and an analog switch can be constituted from a very easy circuit, and do not almost have static power consumption. Moreover, a decoder and an analog switch are arranged instead of a D/A conversion circuit and an operational amplifier like [in the digital drive using organic electroluminescence] drawing 5 . If digital gradation means of displaying is applied to especially organic electroluminescence and even the current variation to a binary fixed electrical potential difference will be stopped even if the current-voltage characteristic of a pixel transistor varies somewhat, there is an advantage that the good image which brightness nonuniformity does not produce can be offered. In addition, a scan side is constituted by the shift register circuit for scanning sequentially like drawing 7 , and is the same as the analog drive of drawing 1010 .

[0011] Next, how to display gradation with the binary fixed electrical potential differences VH and VL is explained with drawing 15 . Dividing the frame period which displays a whole image into two or more subframe periods by which weighting was carried out in time, in each subframe period, in the case of organic electroluminescence, in the case of liquid crystal, it is adding VH or VL to the gate electrode of the 2nd transistor, and it is performing time Pulse Density Modulation to the pixel electrode. Drawing 15 shows the example when the fixed electrical potential difference of the number of bits [the number of subframes and] of input data corresponds with binary, and input data is [the number of 4 bits and subframes] 4. Corresponding to the most significant bit (MSB) of input data - the least significant bit (LSB), subframes SF4-SF1 are assigned, respectively. The combination of the fixed electrical potential differences VH and VL binary [in the subframes SF1-SF4 by which weighting was carried out to the input data] is performing 16 kinds of gradation displays. For example, at the time of "1011", by the subframe SF 3, VL corresponding to [in them] "0" at a binary number is chosen, and VH corresponding to "1" corresponding to [in gradation data] 11 at a decimal number is chosen by subframes SF1, SF2, and SF4. In addition, VH may be corresponded to "0" and VL may be made to correspond to "1" according to the permeability-voltage characteristic (T-V property) of a liquid crystal device, or the luminescence brightness-current characteristic of organic electroluminescence.

[0012] In the conventional digital gradation means of displaying, in order to take the subframe structure by which weighting was carried out in time, as shown in drawing 16 R> 6, it is necessary to choose the scanning line. In order that drawing 16 may scan the scanning line sequentially from a top to the bottom simply and may set time weighting of a subframe to 1:2:4:8 by the case where the number of subframes is 4, the high order bit has the long subframe period. Thus, it sets a horizontal scanning period to H for the number of subframes, setting N and the number of display Rhine as L, and the frame period in the case of scanning sequentially by digital drive is expressed as L

(1+2+4+ ... ** of +2 (N-1)) xH=(Nth power of 2 - 1) HL. If the number N of subframes increases as shown in an upper type, a subframe period will originate in the term of the Nth power of 2, and will become large rapidly. The maintenance period when the subframe period especially over the most significant bit (MSB) does not write in other Rhine will increase very much. A flicker which a frame period increases according to this cause, and is called a flicker arises. Conversely, when frame frequency was set constant, the technical problem that horizontal scan frequency became large and increase of power was caused occurred.

[0013] Next, the animation false profile which is an image quality technical problem peculiar to digital gradation means of displaying is explained. The generating principle of an animation false profile is shown in drawing 17 . A fixed electrical potential difference considers a 2 inter-frame continuous brightness change of a certain pixel supposing a movie display, when the ratio of 4 and the maintenance period of a subframe displays [binary and the number of subframes] 16 gradation by 1:2:4:8. In drawing 17 , in order to give explanation easy, it has chosen sequentially from the subframe SF 4 to the most significant bit in time. At the 1st frame, gradation "7", "0111", is displayed, and suppose that gradation "8", "1000", was displayed by the 2nd frame. [i.e.,] [i.e.,] In this case, "01111000" will be displayed in 2 inter-frame. although a luminescence pattern is accumulated by human being's eyes and it is equalized in time -- frame frequency -- about 60Hz -- "and 1111 ... originally it must be visible to the brightness of "7" or "8" to the luminescence pattern of "-- gradation -- it will be visible to the brightness of "16" for a moment. Thus, the abrupt change of a high order bit brings about an animation false profile. In order to prevent this, generally, the number of subframes is increased and a means to suppress a rapid bit change as much as possible is used. For example, like drawing 18 , the number of subframes is set to 5 and 16 gradation is appropriately chosen for the ratio of the maintenance period of a subframe as 1:2:4:4:4. At this time, the bit change to gradation "gradation from 7"" 8" becomes loose, and the animation false profile about this gradation change decreases. However, the animation false profile to gradation "gradation from 3"" 4" remains. If the number of subframes is increased further, an animation false profile can be reduced further. Thus, when it was going to reduce the animation false profile, the number of subframes needed to be increased, therefore the frame period increased, horizontal scan frequency increased, therefore fixed, then the technical problem that power increase was brought about occurred frame frequency.

[0014]

[Problem(s) to be Solved by the Invention] It will be as follows if the technical problem of the above-mentioned background technique is summarized.

(1) In indicating equipments, such as an indicating equipment used for the pocket device of a small cell drive especially liquid crystal of an active matrix, and organic electroluminescence, when the ******** subframe with weight performed the multi-tone display in time only on the binary fixed electrical potential difference, without using analog circuits, such as a D/A converter and an operational amplifier, the frame period increased, and the flicker was generated and it had become the factor which increases power.

[0015] (2) Moreover, in order to reduce an animation false profile, when the number of subframes was increased, increase of power was caused further.

[0016] The purpose of this invention is offering the active-matrix mold display which performs a multi-tone display by the subframe, moreover shortens a frame period, and prevented generating of a flicker, and its drive approach.

[0017] Moreover, other purposes of this invention are offering the active-matrix mold display which reduced the animation false profile, and its drive approach, without increasing the number of subframes.

[0018]

[Means for Solving the Problem] In the drive approach of an active-matrix mold display of constituting this invention from two or more subframes which write in one frame and consist of a period and a maintenance period, and performing a gradation display by the summation effect of said maintenance period in order to attain the above-mentioned purpose While preparing beforehand two or more signal level fewer than the number of display gradation, choosing the value of either of said two or more signal level according to digital image data and outputting through a signal line At the

maintenance period for every subframe about the one scanning line defined beforehand the scanning line of the remainders other than said one scanning line defined beforehand If a random scan is carried out according to the sequence it was determined beforehand that did not write in the same subframe about the same scanning line and it sees as the whole one-frame period, it will set to each of each scanning line. It is characterized by performing the writing for said two or more subframes of every substantially, securing the maintenance period for every subframe and performing a gradation display drive.

[0019] Both when not circulating with the case where the selection sequence of a subframe period circulates are contained in the selection approach by this invention. Moreover, both the case of sequential scanning and when that is not right are contained about each of a subframe.

[0020] It is effective in the ability to shorten a frame period compared with the conventional digital gradation means of displaying, and reduce a flicker sharply by the above-mentioned configuration.

[0021] Moreover, a horizontal scanning period can enlarge and fixed, then the power by the charge and discharge of the liquid crystal panel capacity carried out to this time amount can be reduced for frame frequency.

[0022] Furthermore, a D/A conversion circuit and an operational amplifier can be unnecessary, the configuration of a drive circuit can be simplified, and reduction of power consumption can be aimed at.

[0023] Moreover, for this invention, the selection sequence of a subframe period is SF1->SF2->... It is ->SFn->SF1->SF2->... There is also a case of the drive approach which chooses the scanning line so that it may circulate with ->SFn. If it is in such a drive approach, as the selection approach of the scanning line, it may not necessarily be scanned sequentially about each of a subframe. Moreover, for this invention, the selection sequence of a subframe period is SF1->SF2->... It is ->SFn->SF1->SF2->... If it circulates with ->SFn and sees about said one subframe period, there is also a case of the drive approach which chooses the scanning line so that it may be scanned sequentially.

[0024] Moreover, this invention is weighting of H and a maintenance period about N and a horizontal scanning period in the number of subframes 1:2:4 : ... When ** (N-1) of :2 and the number of scanning lines are set to L and a positive integer is set to K, said frame period may be set up with NH(1+K (Nth power of 2 - 1)) =NHL, and may be driven.

[0025] moreover, said frame period may be set up with NH(1+sigmaK (i)) =NHL, and this invention may drive it, when weighting of a maintenance period [in / the number of subframes and / for a horizontal scanning period / in it / H and the i-th subframe period] is set to K (i) (however, i= -- referred to as 1, 2, --, N) and the number of scanning lines is set to L [N]

[0026] Moreover, it may set to 2 the degree of freedom of said signal level obtained for said one-frame period to one gradation while this invention prepares beforehand two or more three or more signal level fewer than the number of display gradation, chooses the value of either of said two or more signal level according to digital image data and outputs it through a signal line.

[0027] Two or more signal level is good also as binary, and good also as three or more two or more values. Especially in the case of three or more two or more values (multiple-value-izing), it means performing a gradation display according to concomitant use of digital one and an analog. And when it multiple-value-izes in this way, there is an advantage which can increase the number of display gradation, without increasing the number of subframes. Therefore, if gradation is appropriately chosen so that a rapid bit change with two adjacent gradation may become small, it will become possible to suppress image quality degradation by the animation false profile, without increasing a subframe.

[0028] Moreover, this invention is the active-matrix mold display constituted so that the above-mentioned drive approach might be realized.

[0029] Moreover, as an active-matrix mold display, you may be the liquid crystal display which has a liquid crystal layer, and may be the organic electroluminescence display which replaced with the liquid crystal layer and was equipped with the luminous layer.

[0030]

[Embodiment of the Invention] (Gestalt 1 of operation) Drawing 1 is the important section block diagram of the active matrix liquid crystal display 10 concerning the gestalt 1 of operation, and drawing 2 is the circuit diagram showing the electric configuration of a liquid crystal display 10. In

the liquid crystal display concerning the gestalt 1 of this operation, the same reference mark is given to the part corresponding to the conventional example shown in drawing 10 and drawing 14 , and detailed explanation is omitted. This liquid crystal display 10 is an active-matrix mold display which consists of two or more subframes SF1, SF2, --, SFn (a reference mark SF shows when naming generically) which write in one frame and consist of a period and a maintenance period, and performs a gradation display by the summation effect of a maintenance period. A liquid crystal display 10 has the 1st substrate 11, the 2nd substrate 12 which counters the 1st substrate 11 and is arranged, and a substrate 11 and the liquid crystal layer 103 by which the closure is carried out among 12. Two or more signal lines S1, S2, --, Sn (naming a signal line generically) arranged in the shape of a matrix at the medial surface of the 1st substrate 11 a reference mark S -- being shown -- two or more scanning lines G1, G2, --, Gm (when naming the scanning line generically) Corresponding to each intersection shown by the reference mark G, the storage capacitance 104 connected to the thin film transistor 102 (TFT) as a switching element, the pixel electrode 105 connected to TFT102, and the pixel electrode 105 is formed. Moreover, the counterelectrode 14 is formed in the medial surface of the 2nd substrate 12.

[0031] 20 is a signal-line drive circuit. This signal-line drive circuit 20 has a shift register / latch circuit 106 (for simplification of a drawing, a latch is combined with a shift register and shown as one block), a decoder 501, and an analog switch 502. A decoder 501 and an analog switch 502 constitute an analog multiplexer, and make the work which chooses either of the binary fixed electrical potential differences VH and VL according to digital image data. The function which the signal-line drive circuit 20 prepares beforehand the voltage level of plurality (the gestalt 1 of this operation binary [of the fixed electrical potential differences VH and VL]) smaller than the number of display gradation, chooses the value of either of said two or more voltage levels according to digital image data, and is outputted through a signal line S by such configuration will be achieved.

[0032] Moreover, 30 is a scanning-line drive circuit. This scanning-line drive circuit 30 consists of a decoder 803 which chooses the scanning line G specified by the address signal ADV, and an output buffer 110. The address signal ADV outputted from a control circuit (not shown) is supplied to a decoder 803, and it is constituted so that the scanning line addressed by the address signal ADV may be chosen. In addition, the assignment sequence of the address is beforehand memorized by the memory in a control circuit (not shown), and the random scan of the scanning line will be carried out by the predetermined sequence later mentioned based on this memory.

[0033] Subsequently, the drive approach of a liquid crystal display 10 is explained. With the gestalt 1 of operation, the frame period which displays a whole image is divided into two or more subframe periods by which weighting was carried out in time, and time Pulse Density Modulation is performed by carrying out the selection output of the binary fixed electrical potential differences VH or VL in each subframe period. although the relation of the combination of a fixed electrical potential difference binary [in gradation data and a subframe] is shown in drawing 15 , it differs from drawing 15 -- you may combine and come out.

[0034] Subsequently, a concrete drive sequence is shown in drawing 3 . this drawing 3 -- 0th scanning-line - it is the 16 scanning lines of the 15th scanning line, and a fixed electrical potential difference is binary and the example when both the number of subframes and the number of bits of input gradation data are in agreement by 4 is shown. Drawing 3 (a) and drawing 3 (c) show the subframe of the 0th scanning line. Moreover, drawing 3 (b) and drawing 3 (d) show the selection sequence of the scanning line. In addition, drawing 3 (a) and drawing 3 (c) were drawn by dividing into two in consideration of the tooth space of a drawing etc., although the one-frame period is shown on the whole and drawing 3 (c) follows drawing 3 (a). Moreover, similarly, drawing 3 (b) and drawing 3 (d) were drawn by dividing into two in consideration of the tooth space of a drawing etc., although the one-frame period is shown on the whole and drawing 3 (d) follows drawing 3 (b).

[0035] Hereafter, the concrete drive approach is explained, referring to drawing 3 . The period of each subframes SF1-SF4 consists of a write-in period and a maintenance period, and the write-in period is fixed in every subframe at 1 horizontal-scanning period (1H), and it doubles [period / twice / of 2 / power / the constant of a horizontal scanning] weighting of the maintenance period for every subframe. That is, the maintenance period of a subframe SF 1 is set to 4H, the maintenance period of a subframe SF 2 is set to 8H, the maintenance period of a subframe SF 3 is set to 16H, and

the maintenance period of a subframe SF 4 is set to 32H.
[0036] Here, the drive approach in this invention aims at shortening of a frame period. And the one scanning line beforehand defined for this purpose achievement (in the case of drawing 3) To the maintenance period for every subframe related for being equivalent to the 0th scanning line, it is the scanning line (in the case of drawing 3) of the remainders other than said one scanning line defined beforehand. the 1st - the 15th scanning line -- corresponding, if a random scan is carried out according to the sequence it was determined beforehand that did not write in the same subframe about the same scanning line and it sees as the whole one-frame period It is characterized by securing the writing and maintenance period for every subframe about all the scanning lines, and performing a gradation display.
[0037] Here, it faces setting up the selection sequence of the concrete scanning line for attaining the above-mentioned purpose, and the subframe period is generalized first. When making 1 horizontal-scanning period and N into the total number of subframes and making K into a positive integer for H, it is the i-th subframe period (however, i= 1, 2, ..., N),
(** (i-1) xNK of 1+2) It is expressed xH. The 1st term in the parenthesis of an upper type expresses a write-in period, and the 2nd term expresses the maintenance period. a maintenance period is expressed with x(2 powers) (constant K) x(several subframes N) x (horizontal scanning period H) -- having -- every subframe -- the part of (a power of 2) -- 1, 2, 4, and 8 -- weighting is carried out to ... The term of NK is included at the maintenance period because it is useful to compaction of a frame period so that it may mention later.
[0038] And since it is the sum of all subframe periods, an one-frame period is x(N+NK (1+2+4+ ... ** of +2 (N-1))) H=NH (1+K (Nth power of 2 - 1)).
It is expressed.
[0039] In the wave form chart of drawing 3 (a) and (c), the part of a pulse writes in and a period and the other part are equivalent to a maintenance period.
[0040] By not scanning sequentially from a top to the bottom simply, but choosing in predetermined sequence, as shown in drawing 3 (b) and (d), the selection sequence of the scanning line writes in the subframe of other Rhine using the maintenance period of the subframe period in a high order bit, and is shortening the frame period. The following procedures perform the concrete approach of shortening a frame period.
[0041] (1) In order to write in all subframes, the write-in period of N time is required for the one setting period of the display number of scanning lines to one line. Therefore, when the display number of scanning lines is L, a twice (NxL) as many write-in period as 1 horizontal-scanning period is required for an one-frame period. That is, a write-in period is expressed with NHL. When writing in other Rhine using a maintenance period, the time of NH(1+K (Nth power of 2 - 1)) =NHL being realized is the most efficient. Therefore, it is L=1+K (Nth power of 2 - 1) about the display number of scanning lines.
What is necessary is just to choose so that it may become.
[0042] In the example of drawing 3 (b) and (d), since the number of subframes is N= 4, the display number of scanning lines is set to L=15K+1. K -- a positive integer -- it is -- K= 1, and 2 and 3 -- if ... L= 16, and 31 and 46 -- it becomes ... In drawing 3 (b) and (d), the display number-of-scanning-lines L= 16 or 1-frame period is NHL=64H as K= 1.
[0043] (2) The setting following ** of the selection sequence of the scanning line explains the selection sequence of the scanning line to a detail. Drawing 3 R> 3 is the case where the numbers of subframes are N= 4 and the display number of scanning lines L= 16 (K= 1), and each subframe period is 5H, 9H, 17H, and 33H, and one-frame periods are these sums and are set to 64H. If the 0th top scanning line is observed, the subframe SF 1 to the least significant bit is written in among horizontal scanning period 1H from time of day t= 0. Then, there is a four-H maintenance period and the time of day which writes in SF2 of the 0th scanning line next is set to t=5H. The subframe of other scanning lines is written in between the maintenance periods of this SF1. t=1H [namely,] -- SF2 of the 15th scanning line -- by t=2H, SF4 of the 9th scanning line is written in by t=3H, and SF1 of the 1st scanning line is written in for SF3 of the 13th scanning line t=4H. the sequence of the subframe which will be written in if it puts in another way -- SF1 ->SF2 ->SF3 ->SF4 ->SF1 ... as -- it circulates. Moreover, if one subframe 4, for example, SF, is observed, selection sequence will set

initiation Rhine to 9, and it is 9->10->11->... It is ->15->0->1->... It is scanned sequentially like ->8. It is the same at the point called sequential scanning only by initiation Rhine differing about other subframes. Initiation Rhine of each subframe will be uniquely decided, if the write-in time of day of each subframe to the 0th line is decided. Thus, if the scanning line is chosen so that the subframe of other Rhine may be written in using the maintenance period of a subframe, compared with the case where scan sequentially simply and subframe structure is taken, a frame period can be shortened N/ (Nth power of 2 - 1) twice.

[0044] For example, although drawing 3 and drawing 16 are the same display number of scanning lines and the same number of subframes, the frame period of drawing 16 of sequential scanning can be managed with drawing 3 to being 240H 64H. If a frame period can be shortened, a flicker called a flicker can be prevented and fixed, then the power by the charge and discharge of liquid crystal panel capacity which can increase and perform a horizontal scanning period at this horizontal scanning period can be reduced for frame frequency.

[0045] In the above-mentioned example, although the ratio of the maintenance period of a subframe was set to SF1:SF2:SF3:SF 4= 1:2:4:8, if this invention shows the selection sequence of the scanning line to drawing 4 by the same view as the above even if it is not limited to this and it sets it as SF1:SF2:SF3:SF 4= 2:8:1:4, it can attain shortening of a frame period.

[0046] moreover -- the above-mentioned example -- the selection sequence of a subframe period -- SF1 ->SF2 ->SF3 ->SF4 ->SF1 ... as -- when circulating and seeing about one subframe period, the scanning line was chosen so that it might be scanned sequentially, although it was this invention is not limited to this and shown in drawing 5 -- as -- the selection sequence of a subframe period -- SF1 ->SF2 ->SF3 ->SF4 ->SF1 -- it circulates with ..., also although kicked As long as it sees about one subframe period, it may be made to perform selection which is not scanned sequentially. If it observes in the case of [4] drawing 5 (for example, SF), selection sequence will set initiation Rhine to 3, and it is 3->5->7->9->->11->13->15->2->4->... It is the scan in every two lines like 14->3->5->. It is the scan in every two lines similarly about other Rhine. Even if it is selection of the scanning line shown in such drawing 5 , shortening of a frame period can be attained. In addition, the direction which scans sequentially can simplify the address circuit which specifies the scanning line.

[0047] moreover -- the above-mentioned example -- a subframe period -- the small order of weighting -- SF1->SF2->SF3->SF4->SF1-> ... as -- although it circulated and the scanning line was chosen -- reverse -- descending of weighting -- SF4->SF3->SF2->SF1->SF4-> -- you may circulate with ... or the magnitude of weighting -- not related -- for example, SF3->SF1->SF4->SF2->SF3-> ... as -- subframe sequence may be set up freely.

[0048] Moreover, although the period through which a subframe circulates was made in agreement with N= 4 subframes and made into 4H period in the above-mentioned example, the range of the multiple of N, for example, the case of N= 4, may be circulated 8H period. Moreover, all Rhine may be divided into every block which consists of two or more Rhine, every several lines, and even lines and odd lines, and the sequence of a subframe may be changed. In such a case, it may not necessarily be scanned sequentially about each of a subframe.

[0049] (Epitome of the selection approach of the scanning line) If the selection approach of the above-mentioned scanning line is summarized, it can divide roughly into the following three kinds.

[0050] (1) If the random scan of the scanning line of the remainders other than said one scanning line defined beforehand is carried out to the maintenance period for every subframe about the one scanning line beforehand defined among two or more scanning lines according to the sequence it was determined beforehand that did not write in the same subframe about the same scanning line and it sees as the whole one-frame period, in each of each scanning line, writing / maintenance period for said two or more subframes of every is secured substantially.

[0051] By this selection approach, both when not circulating with the case where the selection sequence of a subframe period circulates are contained. Moreover, both the case of sequential scanning and when that is not right are contained about each of a subframe. According to this selection approach, it is effective in the ability to shorten a frame period by using the holding time effectively.

[0052] (2) The selection sequence of a subframe period is SF1->SF2->... ->SFn->SF1->SF2-> ... The scanning line is chosen so that it may circulate with ->SFn.

[0053] By this selection approach, it may not necessarily be scanned sequentially about each of a subframe. While according to this selection approach being able to use the holding time effectively further and being able to shorten a frame period most compared with the above-mentioned selection approach of (1), it is effective in the ability to simplify the address circuit which specifies the scanning line.
[0054] (3) The selection sequence of a subframe period is SF1->SF2->... ->SFn->SF1->SF2-> ... If it circulates with ->SFn and sees about said one subframe period, the scanning line will be chosen so that it may be scanned sequentially. According to this selection approach, it is effective in the ability to constitute the address circuit which specifies the scanning line from an easy counter circuit of a configuration compared with the selection approach of of above (1) and (2).
[0055] In addition, the selection approach of above-mentioned (1) - (3) may serve as the same drive sequence as a result, although the views of the selection approach of the scanning line differ.
[0056] Moreover, in the above-mentioned example, although the maintenance period of a subframe was made into x(2 powers) (constant K) x(several subframes N) x (horizontal scanning period H), the part of x (2 powers) (constant K) may be set as arbitration. If it becomes common, partial (constant K) x (2 powers) of weight is transposed to K (i), and NH-K (i) is expressed for a maintenance period, and it is the i-th subframe period (however, i= 1, 2, ..., N),
(1+N-K (i)) It can express xH. Moreover, since it is the sum of all subframe periods, an one-frame period is NH(1+K(1)+K (2) + ... +K (N)) =NH (1+sigmaK (i)).
It is expressed. If this is placed with NHL in order to shorten a frame period, the display number of scanning lines will be L=1+K(1) K[+] (2)+... It is +K(N) =1+sigmaK (i).
It becomes. And what is necessary is just to set up the selection sequence of the scanning line based on the view same also in this case as the case x(2 powers) (constant K) x(several subframes N) x (horizontal-scanning period H) Where the maintenance period of the above-mentioned subframe is carried out.
[0057] (Supplementary information of the gestalt 1 of operation) Although the opposite reversal drive was assumed like the conventional example about the alternating current drive of liquid crystal and the fixed electrical potential difference was made binary with the gestalt of ** book operation, when seting opposite constant, a fixed electrical potential difference can be applied by considering as every [the binary one] and a total of four values by straight polarity and negative polarity, respectively. In addition, if the capacity-coupling drive of the preceding paragraph gate or the capacity-coupling drive which controls storage capacitance independently is used, it is possible to carry out opposite for a fixed electrical potential difference to regularity in the binary state.
[0058] ** Although the number of display Rhine was set to L= 16 from N= 4 subframes and a constant K= 1 in this example, this may be the number of maximum Rhine which can be displayed, and the number of Rhine smaller than this is sufficient as it in fact. For example, the number of maximum Rhine which can be displayed is set to L= 16, and when the actually displayed number of Rhine is made into 15 lines, the time amount as which no Rhine is chosen only arises by four [H].
[0059] (Gestalt 2 of operation) Drawing 6 is the circuit diagram showing the electric configuration of liquid crystal display 10A concerning the gestalt 2 of operation. The gestalt 2 of this operation gives the same reference mark to the part which is similar and corresponds to the gestalt 1 of operation. Although the gestalt 1 of the above-mentioned implementation was made to perform a gradation display in the combination of a fixed electrical potential difference binary [in two or more subframes by which weighting was carried out in time], with the gestalt 2 of this operation, the description of constructing the fixed electrical potential difference of three or more values, and performing a gradation display by **** is carried out. This means performing a gradation display according to concomitant use of the gradation display by the multiple-value subframe, i.e., digital one, and an analog.
[0060] Thus, although the circuitry of the analog multiplexer (a decoder and switch) which chooses the fixed electrical potential difference of a signal side drive circuit becomes complicated when it multiple-value-izes, there is an advantage which can increase the number of display gradation, without increasing the number of subframes. for example, the degree of freedom of the fixed electrical potential difference which can be taken to one gradation like drawing 7 when the ratio of a maintenance period is set to 1:2:4:8 by 3 value 4 subframe -- 2, then a maximum of 31 gradation

profit ****.
[0061] It is also possible to lessen the number of subframes by multiple-value-ization on the other hand. for example, the degree of freedom of the fixed electrical potential difference which can be taken to one gradation like drawing 8 when the ratio of a maintenance period is set to 1:2:4 by 3 value 3 subframe -- 2, then a maximum of 15 gradation profit ****. If the number of subframes can be lessened, a frame period can be shortened further and it is possible fixed, then to be able to reduce horizontal scan frequency and to reduce power for frame frequency. In case it multiple-value-izes here, by setting to 2 the degree of freedom of the fixed electrical potential difference which can be taken to one gradation, the brightness jump between adjacent gradation can be prevented and a continuity can be maintained in a gradation-brightness property.
[0062] Moreover, if gradation is appropriately chosen so that a rapid bit change with two adjacent gradation may become small like drawing 9 , using the ratio of a maintenance period as 1:2:2:2 by 3 value 4 subframe, it is possible to suppress image quality degradation by the animation false profile, without increasing a subframe.
[0063] In addition, as well as a binary case when it multiple-value-izes, the alternating current drive of liquid crystal is possible, without doubling the number of fixed electrical potential differences using an opposite reversal drive and a capacity-coupling drive.
[0064] (Other matters) Although the gestalten 1 and 2 of the above-mentioned implementation used and explained liquid crystal to the display device, even if a display device is organic electroluminescence, the selection approach of the scanning line of the gestalten 1 and 2 operation is applicable similarly.
[0065]
[Effect of the Invention] According to this invention, the following effectiveness is done so as mentioned above.
(1) In the conventional active-matrix mold indicating equipment especially liquid crystal, and the active-matrix mold indicating equipment using organic electroluminescence, a frame period can be shortened compared with the conventional digital gradation means of displaying, and it is effective in the ability to reduce a flicker sharply. Moreover, about frame frequency, a horizontal scanning period can enlarge and there are fixed, then effectiveness that the power by the charge and discharge of the liquid crystal panel capacity carried out to this time amount can be reduced.
[0066] (2) A D/A conversion circuit and an operational amplifier are unnecessary, the configuration of a driver circuit can be simplified, and there is effectiveness which can reduce the power consumed by these.
[0067] (3) Don't need the property of a uniform thin film transistor with high degree of accuracy, so that it is required by the conventional analog gradation means of displaying, but it is effective in the ability to reduce image quality degradation of the brightness nonuniformity by transistor-characteristics dispersion etc.
[0068] (4) By multiple-value-izing a fixed electrical potential difference, it becomes possible to prevent image quality degradation of gradation nature, an animation false profile, etc., without increasing power.

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the display which performs a multi-tone display in time in detail with the combination of the voltage level of binary [in a ******** subframe period with weight], or a multiple value, and its drive approach about the display of an active matrix especially liquid crystal, the display that used organic electroluminescence (electroluminescence), and its drive approach.

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PRIOR ART

[Description of the Prior Art] Fewer power consumption is demanded of the display used for the small pocket device by cell drive. Liquid crystal and organic electroluminescence (electroluminescence) are known as a representation rank of the display device which fills such a demand. It is common to control the brightness of a pixel and to perform a gradation display according to the electrical potential difference or current of an analog, in the indicating equipment of an active matrix using these display devices and the indicating equipment which uses the thin film transistor (TFT) of three terminals as a switching element typically. For example, when impressing the electrical potential difference of an analog in the case of liquid crystal, by passing the current of an analog, in the case of organic electroluminescence, the brightness of a display device is changed, and it is indicating by gradation.
[0003] The configuration of the conventional active-matrix liquid crystal panel is shown in drawing 10 , and the gradation method of presentation is explained. 101 is the liquid crystal panel of an active matrix, and consists of signal lines S1-Sn, the scanning lines G1-Gm which intersect perpendicularly with this, and a switching element near [the] the intersection. Si is an example of the thin film transistor (TFT) of a switching element and three common terminals in this case which a certain signal line and Gj have in a certain scanning line, and 102 has near [those] the intersection. 103 shows a liquid crystal device and Counterelectrode Vcom is formed in the side which stands face to face against a transistor 102. 104 is storage capacitance, assisted the capacity component of a liquid crystal device 103, and has prevented degradation of image quality. Common connection of the electrode by the side of the reverse is separately made as Vst in many cases. The intersection 105 by the side of these transistors is equivalent to a pixel electrode.
[0004] If actuation is explained briefly, the scanning line Gj will serve as quantity potential once at an one-frame period, it will be made to flow through a transistor 102, and the pixel electrode 105 103, i.e., liquid crystal capacity, and storage capacitance 104 will be charged to Counterelectrode Vcom to the potential of the signal line Si at this time. The scanning line Gj serves as low voltage after that, a transistor 102 is un-flowing, and this charged potential is maintained during the one-frame period. Moreover, although it is common to carry out an alternating current drive as for liquid crystal, the pulse-like wave which reversed Counterelectrode Vcom and the common electrode Vst of storage capacitance synchronizing with the signal line Si is added, and, generally decreasing the amplitude of a signal line Si is also performed. 106 is a shift register by the side of a signal, and a latch, by the clock signal CKH and start signal STH which are inputted from the outside, carries out the sequential sampling of the video signal, and carries out serial-parallel conversion. In drawing 10 , the example of a digital video signal is shown, a two or more bits video signal is changed into an analog signal by the D/A conversion circuit 107, and current amplification is carried out with an operational amplifier 108, and it is added to signal lines S1-Sn. A scan side consists of the shift register 109 and output buffer 110 which are scanned from a top to the bottom one by one with the clock signal CKV added from the exterior, and a start signal STV, and drives the scanning lines G1-Gm with pulse shape.
[0005] The wave form chart of each part is shown in drawing 11 . HD shows a Horizontal Synchronizing signal, and the period is the horizontal scanning period H, and is equal to the period of above-mentioned STH and above-mentioned CKV. These phases are changed a little with a panel property etc. An input signal is a digital video signal and data change with the period of CKH. FF1,

FF2, and FF3 show the sampling pulse of a signal side shift register. For example, in the case of gradation [4 bits and / 16], if data are expressed in hexadecimals, "F" is sampled and latched to "7" and FF3 by "0" and FF2 at FF1. If D/A conversion of this is carried out to the timing of a latch pulse, the pulse height to the opposite potential Vcom will change, and gradation will be expressed now. If opposite reversal is carried out, in case the alternating current drive of liquid crystal will be carried out, it is possible to set about 1/of voltage swings of a signal line to 2, and, generally it is carried out. in addition, overlapping the preceding paragraph gate (although not shown in drawing Gj- 1), forming the storage capacitance 104 of drawing 10 , impressing a pulse voltage from the gate side of the preceding paragraph, and having kept opposite potential constant -- opposite reversal -- the same -- the voltage swing of a signal line -- about -- there is a capacity-coupling drive which can be reduced to one half (JP,3-35218,A). Or effectiveness with the same said of the case of the capacity-coupling drive (Japanese Patent Application No. 11-255228) which impresses a pulse voltage to storage capacitance independently of the gate is acquired, without making storage capacitance 104 overlap the preceding paragraph gate.

[0006] The selection sequence of the scanning line is shown in drawing 12 . An axis of abscissa is time amount and an axis of ordinate is selection Rhine. The minimum width of face of a time-axis is the horizontal scanning period H, and the number of display Rhine is 16. Like drawing 12 , selection sequence is 0->1->2->... It is scanned sequentially like ->15. Therefore, an one-frame period is completed by 16H, and the writing of the following frame starts. In fact, although a perpendicular blanking period is established at a frame period in addition to the Rhine selection time amount, it is omitting in drawing 12 . In addition, the horizontal scanning period H is equal to the period of HD of drawing 11 , and the analog signal is written in the pixel in this time amount. Next, the configuration of the conventional active-matrix organic EL panel is shown in drawing 13 . The case of the liquid crystal panel of drawing 10 and the thing of this function attach the same number. 401 is the organic EL panel of an active matrix, and consists of signal lines S1-Sn, the scanning lines G1-Gm which intersect perpendicularly with this, and a switching element near [the] the intersection. Si is the 1st and 2nd switching elements which a certain signal line and Gj have in a certain scanning line, and 402 and 403 have near [those] the intersection, and shows the thin film transistor (TFT) of three terminals. 404 is auxiliary capacity and carries out the role holding the electrical potential difference of the signal line Si impressed to the gate electrode of the 2nd transistor 403 through the 1st transistor 402. The location of 405 shows a pixel electrode and is connected to the current supply line Vs through the 2nd transistor 403. 406 is an organic EL device, it is formed between the pixel electrode 405 and Counterelectrode Vcom, emits light according to the current which flows between Counterelectrode Vcom and the electrical-potential-difference supply line Vs, and performs a gradation display by the current control. About actuation of a level drive circuit and a vertical-drive circuit, it is the same as that of the case of the liquid crystal of drawing 1 , and scan the scanning line Gj sequentially, it is made to flow through the 1st transistor 402, and the analog voltage outputted to the signal line Si is written in the 2nd gate and auxiliary capacity 404 of a transistor 403.

[0007] As mentioned above, at a conventional active-matrix liquid crystal panel and a conventional organic EL panel, the gradation display has been performed in modulating brightness in analog. Therefore, the D/A conversion circuit was prepared in the level drive circuit, and the electrical potential difference or current of an analog quantity needed to be outputted to the panel. However, it was the factor in which it is necessary to form an operational amplifier in the latter part of a D/A conversion circuit as a current buffer for carrying out the charge and discharge of the signal-line capacity which is a load, and this increases the power consumption of the whole drive circuit. Because, since a static current flows continuously and is continuing the operational amplifier, even when having not carried out the charge and discharge of the load, and a number equal to the total number of signal lines of operational amplifiers moreover existed, total of the power consumption by the static current of an operational amplifier became large, and this had accounted for the big rate in the power consumption of the whole drive circuit.

[0008] Moreover, in order to control brightness by the gradation display of a active-matrix organic EL panel with the amount of currents which flows to an organic EL device, the display quality of a panel is very sensitive to dispersion in the current-voltage characteristic of a pixel transistor. Therefore, in order to prevent the image quality fall of brightness nonuniformity etc., it is necessary

to form transistor characteristics in homogeneity over the whole panel.
[0009] The drive approach that a time amount modulation performs a gradation display in digital one only using a binary fixed electrical potential difference is learned not using analog circuits, such as a D/A converter and an operational amplifier, as one approach of solving these power technical problems and an image quality technical problem. In this application, this shall be called digital gradation means of displaying. In digital gradation means of displaying, dispersion in the transistor characteristics which there is no power loss by the static current of an analog circuit, and are demanded from high definition is not severe, either.
[0010] The configuration of the conventional digital gradation means of displaying is shown by making the case of liquid crystal into an example at drawing 14 . The analog multiplexer 501, i.e., the decoder, and analog switch 502 with which drawing 14 chooses the binary fixed electrical potential differences VH and VL instead of a D/A conversion circuit and an operational amplifier as compared with drawing 10 are arranged. A decoder and an analog switch can be constituted from a very easy circuit, and do not almost have static power consumption. Moreover, a decoder and an analog switch are arranged instead of a D/A conversion circuit and an operational amplifier like [in the digital drive using organic electroluminescence] drawing 5 . If digital gradation means of displaying is applied to especially organic electroluminescence and even the current variation to a binary fixed electrical potential difference will be stopped even if the current-voltage characteristic of a pixel transistor varies somewhat, there is an advantage that the good image which brightness nonuniformity does not produce can be offered. In addition, a scan side is constituted by the shift register circuit for scanning sequentially like drawing 7 , and is the same as the analog drive of drawing 1010 .
[0011] Next, how to display gradation with the binary fixed electrical potential differences VH and VL is explained with drawing 15 . Dividing the frame period which displays a whole image into two or more subframe periods by which weighting was carried out in time, in each subframe period, in the case of organic electroluminescence, in the case of liquid crystal, it is adding VH or VL to the gate electrode of the 2nd transistor, and it is performing time Pulse Density Modulation to the pixel electrode. Drawing 15 shows the example when the fixed electrical potential difference of the number of bits [the number of subframes and] of input data corresponds with binary, and input data is [the number of 4 bits and subframes] 4. Corresponding to the most significant bit (MSB) of input data - the least significant bit (LSB), subframes SF4-SF1 are assigned, respectively. The combination of the fixed electrical potential differences VH and VL binary [in the subframes SF1-SF4 by which weighting was carried out to the input data] is performing 16 kinds of gradation displays. For example, at the time of "1011", by the subframe SF 3, VL corresponding to [in them] "0" at a binary number is chosen, and VH corresponding to "1" corresponding to [in gradation data] 11 at a decimal number is chosen by subframes SF1, SF2, and SF4. In addition, VH may be corresponded to "0" and VL may be made to correspond to "1" according to the permeability-voltage characteristic (T-V property) of a liquid crystal device, or the luminescence brightness-current characteristic of organic electroluminescence.
[0012] In the conventional digital gradation means of displaying, in order to take the subframe structure by which weighting was carried out in time, as shown in drawing 16 R> 6, it is necessary to choose the scanning line. In order that drawing 16 may scan the scanning line sequentially from a top to the bottom simply and may set time weighting of a subframe to 1:2:4:8 by the case where the number of subframes is 4, the high order bit has the long subframe period. Thus, it sets a horizontal scanning period to H for the number of subframes, setting N and the number of display Rhine as L, and the frame period in the case of scanning sequentially by digital drive is expressed as L (1+2+4+ ... ** of +2 (N-1)) xH=(Nth power of 2 - 1) HL. If the number N of subframes increases as shown in an upper type, a subframe period will originate in the term of the Nth power of 2, and will become large rapidly. The maintenance period when the subframe period especially over the most significant bit (MSB) does not write in other Rhine will increase very much. A flicker which a frame period increases according to this cause, and is called a flicker arises. Conversely, when frame frequency was set constant, the technical problem that horizontal scan frequency became large and increase of power was caused occurred.
[0013] Next, the animation false profile which is an image quality technical problem peculiar to

digital gradation means of displaying is explained. The generating principle of an animation false profile is shown in drawing 17 . A fixed electrical potential difference considers a 2 inter-frame continuous brightness change of a certain pixel supposing a movie display, when the ratio of 4 and the maintenance period of a subframe displays [binary and the number of subframes] 16 gradation by 1:2:4:8. In drawing 17 , in order to give explanation easy, it has chosen sequentially from the subframe SF 4 to the most significant bit in time. At the 1st frame, gradation "7", "0111", is displayed, and suppose that gradation "8", "1000", was displayed by the 2nd frame. [i.e.,] [i.e.,] In this case, "01111000" will be displayed in 2 inter-frame. although a luminescence pattern is accumulated by human being's eyes and it is equalized in time -- frame frequency -- about 60Hz -- "and 1111 ... originally it must be visible to the brightness of "7" or "8" to the luminescence pattern of "-- gradation -- it will be visible to the brightness of "16" for a moment. Thus, the abrupt change of a high order bit brings about an animation false profile. In order to prevent this, generally, the number of subframes is increased and a means to suppress a rapid bit change as much as possible is used. For example, like drawing 18 , the number of subframes is set to 5 and 16 gradation is appropriately chosen for the ratio of the maintenance period of a subframe as 1:2:4:4:4. At this time, the bit change to gradation "gradation from 7"" 8" becomes loose, and the animation false profile about this gradation change decreases. However, the animation false profile to gradation "gradation from 3"" 4" remains. If the number of subframes is increased further, an animation false profile can be reduced further. Thus, when it was going to reduce the animation false profile, the number of subframes needed to be increased, therefore the frame period increased, horizontal scan frequency increased, therefore fixed, then the technical problem that power increase was brought about occurred frame frequency.

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EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, the following effectiveness is done so as mentioned above.
(1) In the conventional active-matrix mold indicating equipment especially liquid crystal, and the active-matrix mold indicating equipment using organic electroluminescence, a frame period can be shortened compared with the conventional digital gradation means of displaying, and it is effective in the ability to reduce a flicker sharply. Moreover, about frame frequency, a horizontal scanning period can enlarge and there are fixed, then effectiveness that the power by the charge and discharge of the liquid crystal panel capacity carried out to this time amount can be reduced.
[0066] (2) A D/A conversion circuit and an operational amplifier are unnecessary, the configuration of a driver circuit can be simplified, and there is effectiveness which can reduce the power consumed by these.
[0067] (3) Don't need the property of a uniform thin film transistor with high degree of accuracy, so that it is required by the conventional analog gradation means of displaying, but it is effective in the ability to reduce image quality degradation of the brightness nonuniformity by transistor-characteristics dispersion etc.
[0068] (4) By multiple-value-izing a fixed electrical potential difference, it becomes possible to prevent image quality degradation of gradation nature, an animation false profile, etc., without increasing power.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] It will be as follows if the technical problem of the above-mentioned background technique is summarized.
(1) In indicating equipments, such as an indicating equipment used for the pocket device of a small cell drive especially liquid crystal of an active matrix, and organic electroluminescence, when the ******** subframe with weight performed the multi-tone display in time only on the binary fixed electrical potential difference, without using analog circuits, such as a D/A converter and an operational amplifier, the frame period increased, and the flicker was generated and it had become the factor which increases power.
[0015] (2) Moreover, in order to reduce an animation false profile, when the number of subframes was increased, increase of power was caused further.
[0016] The purpose of this invention is offering the active-matrix mold display which performs a multi-tone display by the subframe, moreover shortens a frame period, and prevented generating of a flicker, and its drive approach.
[0017] Moreover, other purposes of this invention are offering the active-matrix mold display which reduced the animation false profile, and its drive approach, without increasing the number of subframes.

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MEANS

[Means for Solving the Problem] In the drive approach of an active-matrix mold display of constituting this invention from two or more subframes which write in one frame and consist of a period and a maintenance period, and performing a gradation display by the summation effect of said maintenance period in order to attain the above-mentioned purpose While preparing beforehand two or more signal level fewer than the number of display gradation, choosing the value of either of said two or more signal level according to digital image data and outputting through a signal line At the maintenance period for every subframe about the one scanning line defined beforehand the scanning line of the remainders other than said one scanning line defined beforehand If a random scan is carried out according to the sequence it was determined beforehand that did not write in the same subframe about the same scanning line and it sees as the whole one-frame period, it will set to each of each scanning line. It is characterized by performing the writing for said two or more subframes of every substantially, securing the maintenance period for every subframe and performing a gradation display drive.
[0019] Both when not circulating with the case where the selection sequence of a subframe period circulates are contained in the selection approach by this invention. Moreover, both the case of sequential scanning and when that is not right are contained about each of a subframe.
[0020] It is effective in the ability to shorten a frame period compared with the conventional digital gradation means of displaying, and reduce a flicker sharply by the above-mentioned configuration.
[0021] Moreover, a horizontal scanning period can enlarge and fixed, then the power by the charge and discharge of the liquid crystal panel capacity carried out to this time amount can be reduced for frame frequency.
[0022] Furthermore, a D/A conversion circuit and an operational amplifier can be unnecessary, the configuration of a drive circuit can be simplified, and reduction of power consumption can be aimed at.
[0023] Moreover, for this invention, the selection sequence of a subframe period is SF1->SF2->... It is ->SFn->SF1->SF2->... There is also a case of the drive approach which chooses the scanning line so that it may circulate with ->SFn. If it is in such a drive approach, as the selection approach of the scanning line, it may not necessarily be scanned sequentially about each of a subframe. Moreover, for this invention, the selection sequence of a subframe period is SF1->SF2->... It is ->SFn->SF1->SF2->... If it circulates with ->SFn and sees about said one subframe period, there is also a case of the drive approach which chooses the scanning line so that it may be scanned sequentially.
[0024] Moreover, this invention is weighting of H and a maintenance period about N and a horizontal scanning period in the number of subframes 1:2:4 : ... When ** (N-1) of :2 and the number of scanning lines are set to L and a positive integer is set to K, said frame period may be set up with NH(1+K (Nth power of 2 - 1)) =NHL, and may be driven.
[0025] moreover, said frame period may be set up with NH(1+sigmaK (i)) =NHL, and this invention may drive it, when weighting of a maintenance period [in / the number of subframes and / for a horizontal scanning period / in it / H and the i-th subframe period] is set to K (i) (however, i= -- referred to as 1, 2, --, N) and the number of scanning lines is set to L [N]
[0026] Moreover, it may set to 2 the degree of freedom of said signal level obtained for said one-frame period to one gradation while this invention prepares beforehand two or more three or more signal level fewer than the number of display gradation, chooses the value of either of said two or

more signal level according to digital image data and outputs it through a signal line.
[0027] Two or more signal level is good also as binary, and good also as three or more two or more values. Especially in the case of three or more two or more values (multiple-value-izing), it means performing a gradation display according to concomitant use of digital one and an analog. And when it multiple-value-izes in this way, there is an advantage which can increase the number of display gradation, without increasing the number of subframes. Therefore, if gradation is appropriately chosen so that a rapid bit change with two adjacent gradation may become small, it will become possible to suppress image quality degradation by the animation false profile, without increasing a subframe.
[0028] Moreover, this invention is the active-matrix mold display constituted so that the above-mentioned drive approach might be realized.
[0029] Moreover, as an active-matrix mold display, you may be the liquid crystal display which has a liquid crystal layer, and may be the organic electroluminescence display which replaced with the liquid crystal layer and was equipped with the luminous layer.
[0030]
[Embodiment of the Invention] (Gestalt 1 of operation) Drawing 1 is the important section block diagram of the active matrix liquid crystal display 10 concerning the gestalt 1 of operation, and drawing 2 is the circuit diagram showing the electric configuration of a liquid crystal display 10. In the liquid crystal display concerning the gestalt 1 of this operation, the same reference mark is given to the part corresponding to the conventional example shown in drawing 10 and drawing 14 , and detailed explanation is omitted. This liquid crystal display 10 is an active-matrix mold display which consists of two or more subframes SF1, SF2, --, SFn (a reference mark SF shows when naming generically) which write in one frame and consist of a period and a maintenance period, and performs a gradation display by the summation effect of a maintenance period. A liquid crystal display 10 has the 1st substrate 11, the 2nd substrate 12 which counters the 1st substrate 11 and is arranged, and a substrate 11 and the liquid crystal layer 103 by which the closure is carried out among 12. Two or more signal lines S1, S2, --, Sn (naming a signal line generically) arranged in the shape of a matrix at the medial surface of the 1st substrate 11 a reference mark S -- being shown -- two or more scanning lines G1, G2, --, Gm (when naming the scanning line generically) Corresponding to each intersection shown by the reference mark G, the storage capacitance 104 connected to the thin film transistor 102 (TFT) as a switching element, the pixel electrode 105 connected to TFT102, and the pixel electrode 105 is formed. Moreover, the counterelectrode 14 is formed in the medial surface of the 2nd substrate 12.
[0031] 20 is a signal-line drive circuit. This signal-line drive circuit 20 has a shift register / latch circuit 106 (for simplification of a drawing, a latch is combined with a shift register and shown as one block), a decoder 501, and an analog switch 502. A decoder 501 and an analog switch 502 constitute an analog multiplexer, and make the work which chooses either of the binary fixed electrical potential differences VH and VL according to digital image data. The function which the signal-line drive circuit 20 prepares beforehand the voltage level of plurality (the gestalt 1 of this operation binary [of the fixed electrical potential differences VH and VL]) smaller than the number of display gradation, chooses the value of either of said two or more voltage levels according to digital image data, and is outputted through a signal line S by such configuration will be achieved.
[0032] Moreover, 30 is a scanning-line drive circuit. This scanning-line drive circuit 30 consists of a decoder 803 which chooses the scanning line G specified by the address signal ADV, and an output buffer 110. The address signal ADV outputted from a control circuit (not shown) is supplied to a decoder 803, and it is constituted so that the scanning line addressed by the address signal ADV may be chosen. In addition, the assignment sequence of the address is beforehand memorized by the memory in a control circuit (not shown), and the random scan of the scanning line will be carried out by the predetermined sequence later mentioned based on this memory.
[0033] Subsequently, the drive approach of a liquid crystal display 10 is explained. With the gestalt 1 of operation, the frame period which displays a whole image is divided into two or more subframe periods by which weighting was carried out in time, and time Pulse Density Modulation is performed by carrying out the selection output of the binary fixed electrical potential differences VH or VL in each subframe period. although the relation of the combination of a fixed electrical potential

difference binary [in gradation data and a subframe] is shown in drawing 15 , it differs from drawing 15 -- you may combine and come out.
[0034] Subsequently, a concrete drive sequence is shown in drawing 3 . this drawing 3 -- 0th scanning-line - it is the 16 scanning lines of the 15th scanning line, and a fixed electrical potential difference is binary and the example when both the number of subframes and the number of bits of input gradation data are in agreement by 4 is shown. Drawing 3 (a) and drawing 3 (c) show the subframe of the 0th scanning line. Moreover, drawing 3 (b) and drawing 3 (d) show the selection sequence of the scanning line. In addition, drawing 3 (a) and drawing 3 (c) were drawn by dividing into two in consideration of the tooth space of a drawing etc., although the one-frame period is shown on the whole and drawing 3 (c) follows drawing 3 (a). Moreover, similarly, drawing 3 (b) and drawing 3 (d) were drawn by dividing into two in consideration of the tooth space of a drawing etc., although the one-frame period is shown on the whole and drawing 3 (d) follows drawing 3 (b).
[0035] Hereafter, the concrete drive approach is explained, referring to drawing 3 . The period of each subframes SF1-SF4 consists of a write-in period and a maintenance period, and the write-in period is fixed in every subframe at 1 horizontal-scanning period (1H), and it doubles [period / twice / of 2 / power / the constant of a horizontal scanning] weighting of the maintenance period for every subframe. That is, the maintenance period of a subframe SF 1 is set to 4H, the maintenance period of a subframe SF 2 is set to 8H, the maintenance period of a subframe SF 3 is set to 16H, and the maintenance period of a subframe SF 4 is set to 32H.
[0036] Here, the drive approach in this invention aims at shortening of a frame period. And the one scanning line beforehand defined for this purpose achievement (in the case of drawing 3) To the maintenance period for every subframe related for being equivalent to the 0th scanning line, it is the scanning line (in the case of drawing 3) of the remainders other than said one scanning line defined beforehand. the 1st - the 15th scanning line -- corresponding, if a random scan is carried out according to the sequence it was determined beforehand that did not write in the same subframe about the same scanning line and it sees as the whole one-frame period It is characterized by securing the writing and maintenance period for every subframe about all the scanning lines, and performing a gradation display.
[0037] Here, it faces setting up the selection sequence of the concrete scanning line for attaining the above-mentioned purpose, and the subframe period is generalized first. When making 1 horizontal-scanning period and N into the total number of subframes and making K into a positive integer for H, it is the i-th subframe period (however, i= 1, 2, ..., N),
(** (i-1) xNK of 1+2) It is expressed xH. The 1st term in the parenthesis of an upper type expresses a write-in period, and the 2nd term expresses the maintenance period. a maintenance period is expressed with x(2 powers) (constant K) x(several subframes N) x (horizontal scanning period H) -- having -- every subframe -- the part of (a power of 2) -- 1, 2, 4, and 8 -- weighting is carried out to ... The term of NK is included at the maintenance period because it is useful to compaction of a frame period so that it may mention later.
[0038] And since it is the sum of all subframe periods, an one-frame period is x(N+NK (1+2+4+ ... ** of +2 (N-1))) H=NH (1+K (Nth power of 2 - 1)).
It is expressed.
[0039] In the wave form chart of drawing 3 (a) and (c), the part of a pulse writes in and a period and the other part are equivalent to a maintenance period.
[0040] By not scanning sequentially from a top to the bottom simply, but choosing in predetermined sequence, as shown in drawing 3 (b) and (d), the selection sequence of the scanning line writes in the subframe of other Rhine using the maintenance period of the subframe period in a high order bit, and is shortening the frame period. The following procedures perform the concrete approach of shortening a frame period.
[0041] (1) In order to write in all subframes, the write-in period of N time is required for the one setting period of the display number of scanning lines to one line. Therefore, when the display number of scanning lines is L, a twice (NxL) as many write-in period as 1 horizontal-scanning period is required for an one-frame period. That is, a write-in period is expressed with NHL. When writing in other Rhine using a maintenance period, the time of NH(1+K (Nth power of 2 - 1)) =NHL being realized is the most efficient. Therefore, it is L=1+K (Nth power of 2 - 1) about the display

number of scanning lines.
What is necessary is just to choose so that it may become.
[0042] In the example of drawing 3 (b) and (d), since the number of subframes is N= 4, the display number of scanning lines is set to L=15K+1. K -- a positive integer -- it is -- K= 1, and 2 and 3 -- if ... L= 16, and 31 and 46 -- it becomes ... In drawing 3 (b) and (d), the display number-of-scanning-lines L= 16 or 1-frame period is NHL=64H as K= 1.
[0043] (2) The setting following ** of the selection sequence of the scanning line explains the selection sequence of the scanning line to a detail. Drawing 3 R> 3 is the case where the numbers of subframes are N= 4 and the display number of scanning lines L= 16 (K= 1), and each subframe period is 5H, 9H, 17H, and 33H, and one-frame periods are these sums and are set to 64H. If the 0th top scanning line is observed, the subframe SF 1 to the least significant bit is written in among horizontal scanning period 1H from time of day t= 0. Then, there is a four-H maintenance period and the time of day which writes in SF2 of the 0th scanning line next is set to t=5H. The subframe of other scanning lines is written in between the maintenance periods of this SF1. t=1H [namely,] -- SF2 of the 15th scanning line -- by t=2H, SF4 of the 9th scanning line is written in by t=3H, and SF1 of the 1st scanning line is written in for SF3 of the 13th scanning line t=4H. the sequence of the subframe which will be written in if it puts in another way -- SF1 ->SF2 ->SF3 ->SF4 ->SF1 ... as -- it circulates. Moreover, if one subframe 4, for example, SF, is observed, selection sequence will set initiation Rhine to 9, and it is 9->10->11->... It is ->15->0->1->... It is scanned sequentially like ->8. It is the same at the point called sequential scanning only by initiation Rhine differing about other subframes. Initiation Rhine of each subframe will be uniquely decided, if the write-in time of day of each subframe to the 0th line is decided. Thus, if the scanning line is chosen so that the subframe of other Rhine may be written in using the maintenance period of a subframe, compared with the case where scan sequentially simply and subframe structure is taken, a frame period can be shortened N/ (Nth power of 2 - 1) twice.
[0044] For example, although drawing 3 and drawing 16 are the same display number of scanning lines and the same number of subframes, the frame period of drawing 16 of sequential scanning can be managed with drawing 3 to being 240H 64H. If a frame period can be shortened, a flicker called a flicker can be prevented and fixed, then the power by the charge and discharge of liquid crystal panel capacity which can increase and perform a horizontal scanning period at this horizontal scanning period can be reduced for frame frequency.
[0045] In the above-mentioned example, although the ratio of the maintenance period of a subframe was set to SF1:SF2:SF3:SF 4= 1:2:4:8, if this invention shows the selection sequence of the scanning line to drawing 4 by the same view as the above even if it is not limited to this and it sets it as SF1:SF2:SF3:SF 4= 2:8:1:4, it can attain shortening of a frame period.
[0046] moreover -- the above-mentioned example -- the selection sequence of a subframe period -- SF1 ->SF2 ->SF3 ->SF4 ->SF1 ... as -- when circulating and seeing about one subframe period, the scanning line was chosen so that it might be scanned sequentially, although it was this invention is not limited to this and shown in drawing 5 -- as -- the selection sequence of a subframe period -- SF1 ->SF2 ->SF3 ->SF4 ->SF1 -- it circulates with ..., also although kicked As long as it sees about one subframe period, it may be made to perform selection which is not scanned sequentially. If it observes in the case of [4] drawing 5 (for example, SF), selection sequence will set initiation Rhine to 3, and it is 3->5->7->9->->11->13->15->2->4->... It is the scan in every two lines like 14->3->5->. It is the scan in every two lines similarly about other Rhine. Even if it is selection of the scanning line shown in such drawing 5 , shortening of a frame period can be attained. In addition, the direction which scans sequentially can simplify the address circuit which specifies the scanning line.
[0047] moreover -- the above-mentioned example -- a subframe period -- the small order of weighting -- SF1->SF2->SF3->SF4->SF1-> ... as -- although it circulated and the scanning line was chosen -- reverse -- descending of weighting -- SF4->SF3->SF2->SF1->SF4-> -- you may circulate with ... or the magnitude of weighting -- not related -- for example, SF3->SF1->SF4->SF2->SF3-> ... as -- subframe sequence may be set up freely.
[0048] Moreover, although the period through which a subframe circulates was made in agreement with N= 4 subframes and made into 4H period in the above-mentioned example, the range of the multiple of N, for example, the case of N= 4, may be circulated 8H period. Moreover, all Rhine may

be divided into every block which consists of two or more Rhine, every several lines, and even lines and odd lines, and the sequence of a subframe may be changed. In such a case, it may not necessarily be scanned sequentially about each of a subframe.
[0049] (Epitome of the selection approach of the scanning line) If the selection approach of the above-mentioned scanning line is summarized, it can divide roughly into the following three kinds.
[0050] (1) If the random scan of the scanning line of the remainders other than said one scanning line defined beforehand is carried out to the maintenance period for every subframe about the one scanning line beforehand defined among two or more scanning lines according to the sequence it was determined beforehand that did not write in the same subframe about the same scanning line and it sees as the whole one-frame period, in each of each scanning line, writing / maintenance period for said two or more subframes of every is secured substantially.
[0051] By this selection approach, both when not circulating with the case where the selection sequence of a subframe period circulates are contained. Moreover, both the case of sequential scanning and when that is not right are contained about each of a subframe. According to this selection approach, it is effective in the ability to shorten a frame period by using the holding time effectively.
[0052] (2) The selection sequence of a subframe period is SF1->SF2->... ->SFn->SF1->SF2-> ... The scanning line is chosen so that it may circulate with ->SFn.
[0053] By this selection approach, it may not necessarily be scanned sequentially about each of a subframe. While according to this selection approach being able to use the holding time effectively further and being able to shorten a frame period most compared with the above-mentioned selection approach of (1), it is effective in the ability to simplify the address circuit which specifies the scanning line.
[0054] (3) The selection sequence of a subframe period is SF1->SF2->... ->SFn->SF1->SF2-> ... If it circulates with ->SFn and sees about said one subframe period, the scanning line will be chosen so that it may be scanned sequentially. According to this selection approach, it is effective in the ability to constitute the address circuit which specifies the scanning line from an easy counter circuit of a configuration compared with the selection approach of of above (1) and (2).
[0055] In addition, the selection approach of above-mentioned (1) - (3) may serve as the same drive sequence as a result, although the views of the selection approach of the scanning line differ.
[0056] Moreover, in the above-mentioned example, although the maintenance period of a subframe was made into x(2 powers) (constant K) x(several subframes N) x (horizontal scanning period H), the part of x (2 powers) (constant K) may be set as arbitration. If it becomes common, partial (constant K) x (2 powers) of weight is transposed to K (i), and NH-K (i) is expressed for a maintenance period, and it is the i-th subframe period (however, i= 1, 2, ..., N),
(1+N-K (i)) It can express xH. Moreover, since it is the sum of all subframe periods, an one-frame period is NH(1+K(1)+K (2) + ... +K (N)) =NH (1+sigmaK (i)).
It is expressed. If this is placed with NHL in order to shorten a frame period, the display number of scanning lines will be L=1+K(1) K[+] (2)+... It is +K(N) =1+sigmaK (i).
It becomes. And what is necessary is just to set up the selection sequence of the scanning line based on the view same also in this case as the case x(2 powers) (constant K) x(several subframes N) x (horizontal-scanning period H) Where the maintenance period of the above-mentioned subframe is carried out.
[0057] (Supplementary information of the gestalt 1 of operation) Although the opposite reversal drive was assumed like the conventional example about the alternating current drive of liquid crystal and the fixed electrical potential difference was made binary with the gestalt of ** book operation, when seting opposite constant, a fixed electrical potential difference can be applied by considering as every [the binary one] and a total of four values by straight polarity and negative polarity, respectively. In addition, if the capacity-coupling drive of the preceding paragraph gate or the capacity-coupling drive which controls storage capacitance independently is used, it is possible to carry out opposite for a fixed electrical potential difference to regularity in the binary state.
[0058] ** Although the number of display Rhine was set to L= 16 from N= 4 subframes and a constant K= 1 in this example, this may be the number of maximum Rhine which can be displayed, and the number of Rhine smaller than this is sufficient as it in fact. For example, the number of

maximum Rhine which can be displayed is set to L= 16, and when the actually displayed number of Rhine is made into 15 lines, the time amount as which no Rhine is chosen only arises by four [H].
[0059] (Gestalt 2 of operation) Drawing 6 is the circuit diagram showing the electric configuration of liquid crystal display 10A concerning the gestalt 2 of operation. The gestalt 2 of this operation gives the same reference mark to the part which is similar and corresponds to the gestalt 1 of operation. Although the gestalt 1 of the above-mentioned implementation was made to perform a gradation display in the combination of a fixed electrical potential difference binary [in two or more subframes by which weighting was carried out in time], with the gestalt 2 of this operation, the description of constructing the fixed electrical potential difference of three or more values, and performing a gradation display by **** is carried out. This means performing a gradation display according to concomitant use of the gradation display by the multiple-value subframe, i.e., digital one, and an analog.
[0060] Thus, although the circuitry of the analog multiplexer (a decoder and switch) which chooses the fixed electrical potential difference of a signal side drive circuit becomes complicated when it multiple-value-izes, there is an advantage which can increase the number of display gradation, without increasing the number of subframes. for example, the degree of freedom of the fixed electrical potential difference which can be taken to one gradation like drawing 7 when the ratio of a maintenance period is set to 1:2:4:8 by 3 value 4 subframe -- 2, then a maximum of 31 gradation profit ****.
[0061] It is also possible to lessen the number of subframes by multiple-value-ization on the other hand. for example, the degree of freedom of the fixed electrical potential difference which can be taken to one gradation like drawing 8 when the ratio of a maintenance period is set to 1:2:4 by 3 value 3 subframe -- 2, then a maximum of 15 gradation profit ****. If the number of subframes can be lessened, a frame period can be shortened further and it is possible fixed, then to be able to reduce horizontal scan frequency and to reduce power for frame frequency. In case it multiple-value-izes here, by setting to 2 the degree of freedom of the fixed electrical potential difference which can be taken to one gradation, the brightness jump between adjacent gradation can be prevented and a continuity can be maintained in a gradation-brightness property.
[0062] Moreover, if gradation is appropriately chosen so that a rapid bit change with two adjacent gradation may become small like drawing 9 , using the ratio of a maintenance period as 1:2:2:2 by 3 value 4 subframe, it is possible to suppress image quality degradation by the animation false profile, without increasing a subframe.
[0063] In addition, as well as a binary case when it multiple-value-izes, the alternating current drive of liquid crystal is possible, without doubling the number of fixed electrical potential differences using an opposite reversal drive and a capacity-coupling drive.
[0064] (Other matters) Although the gestalten 1 and 2 of the above-mentioned implementation used and explained liquid crystal to the display device, even if a display device is organic electroluminescence, the selection approach of the scanning line of the gestalten 1 and 2 operation is applicable similarly.

[Translation done.]

* NOTICES *

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3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the important section block diagram of the active matrix liquid crystal display 10 concerning the gestalt 1 of operation.
[Drawing 2] It is the circuit diagram showing the electric configuration of a liquid crystal display 10.

[Drawing 3] It is the drive sequence diagram showing the selection sequence of the scanning line in the gestalt 1 of operation.
[Drawing 4] It is the drive sequence diagram showing the modification of the selection sequence of the scanning line in the gestalt 1 of operation.
[Drawing 5] It is the drive sequence diagram showing the modification of the selection sequence of the scanning line in the gestalt 1 of operation.
[Drawing 6] It is the circuit diagram showing the electric configuration of liquid crystal display 10A concerning the gestalt 2 of operation.
[Drawing 7] It is drawing showing the relation of the gradation and the subframe in the gestalt 2 of operation.
[Drawing 8] It is drawing showing the modification of the relation of the gradation and the subframe in the gestalt 2 of operation.
[Drawing 9] It is drawing showing the modification of the relation of the gradation and the subframe in the gestalt 2 of operation.
[Drawing 10] It is the block diagram of the analog gradation display in the conventional active-matrix liquid crystal panel.
[Drawing 11] It is the wave form chart of the analog gradation display in the conventional active-matrix liquid crystal panel.
[Drawing 12] It is drawing showing the scanning-line selection sequence of the conventional analog gradation display.
[Drawing 13] It is the block diagram of the analog gradation display in the conventional active-matrix organic EL panel.
[Drawing 14] It is the block diagram of the digital gradation display in the conventional active-matrix liquid crystal panel.
[Drawing 15] It is drawing showing the relation between the gradation in a digital gradation display, and a subframe.
[Drawing 16] It is drawing showing the scanning-line selection sequence of the conventional digital gradation display.
[Drawing 17] It is drawing showing the generating principle of the animation false profile in a digital gradation display.
[Drawing 18] It is drawing showing the reduction approach of the animation false profile in the conventional digital gradation display.
[Description of Notations]
10 : Liquid Crystal Display
20 : Signal Side Drive Circuit
30 : Scanning-Line Drive Circuit
101: Liquid crystal panel

102,402,403: Switching element
103: Liquid crystal layer
104: Storage capacitance
105,405: Pixel electrode
106: A shift register and a latch
110: Output buffer
401: The organic EL panel of an active matrix
404: Auxiliary capacity
406: Organic EL device
501: Decoder
502: Analog switch
803: Scanning-line selection decoder
S1, S2, S3, Si, Sn: Signal line
G1, G2, G3, Gj, Gm: Scanning line
CKH: Signal side clock signal
STH: Signal side start signal
CKV: Scan side clock signal
STV: Scan side clock signal
ADV: Scan side address signal
Vcom: Counterelectrode
Vst: The common electrode of storage capacitance
Vs: Current supply line
HD: Horizontal Synchronizing signal
FF1, FF2, FF3: The sampling pulse of a signal side shift register
VH, VL, V1, V2, V3: Fixed electrical potential difference
SF1, SF2, SF3, SF4: Subframe period

[Translation done.]

* NOTICES *

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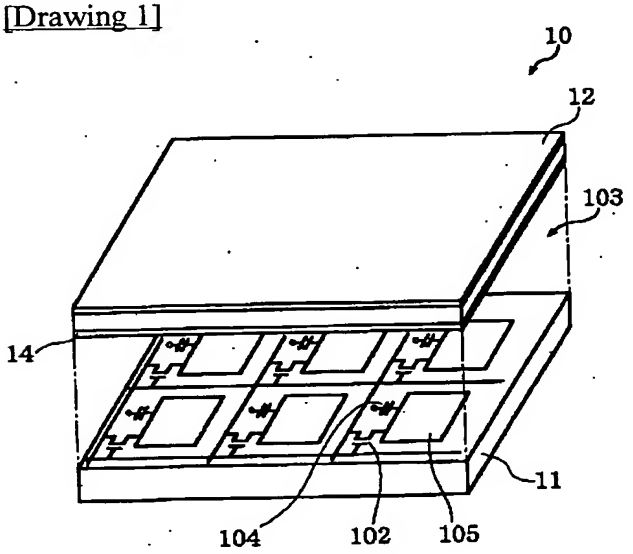
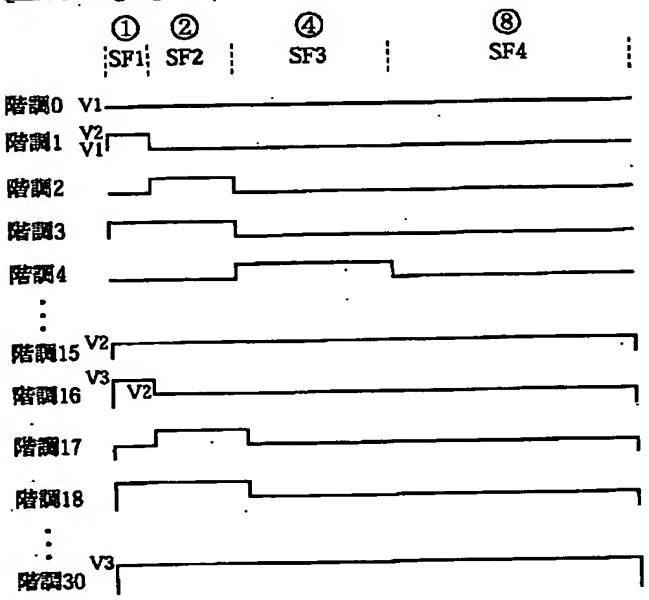
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

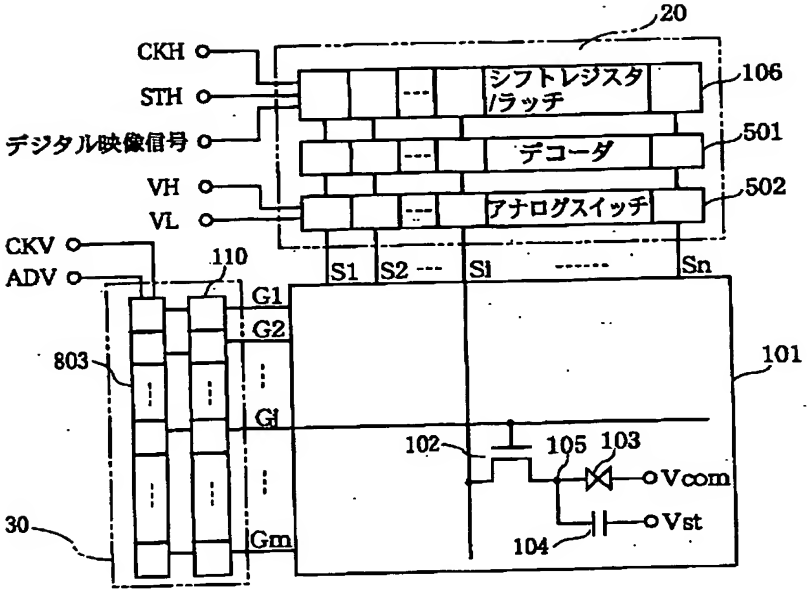
[Drawing 1]



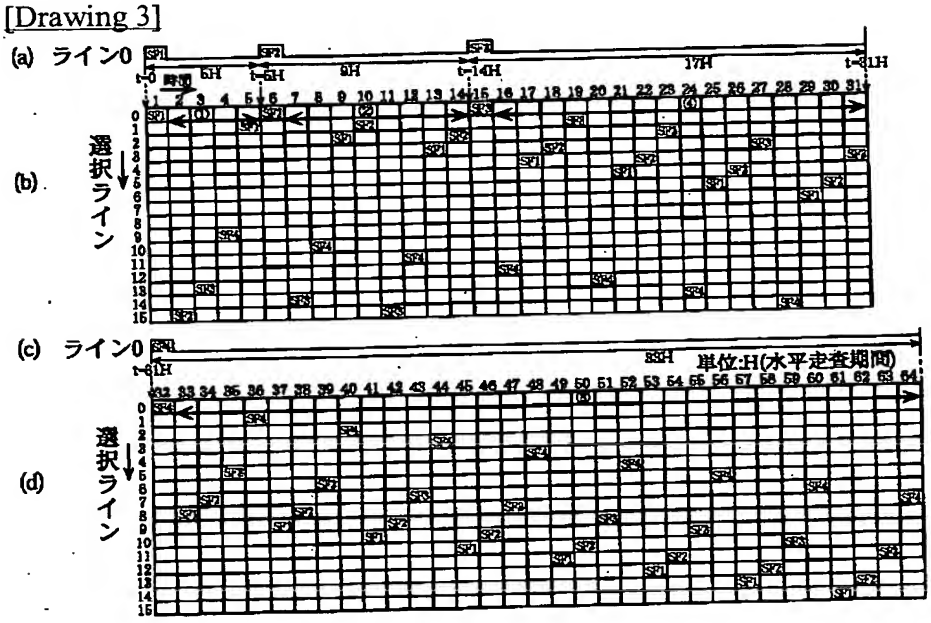
[Drawing 7]



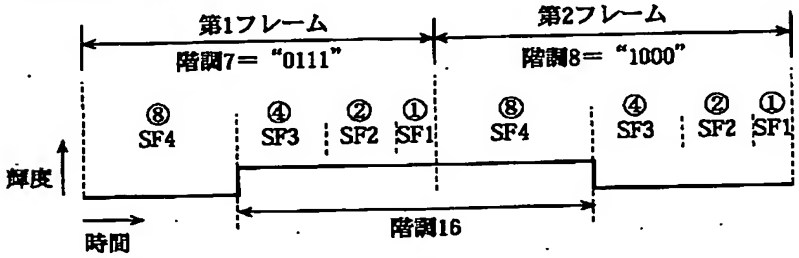
[Drawing 2]



[Drawing 3]



[Drawing 17]



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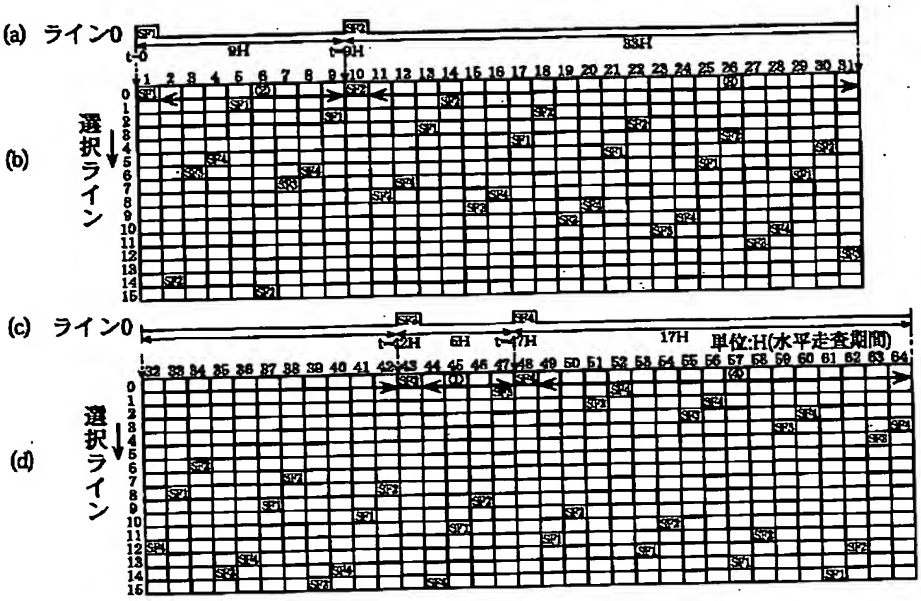

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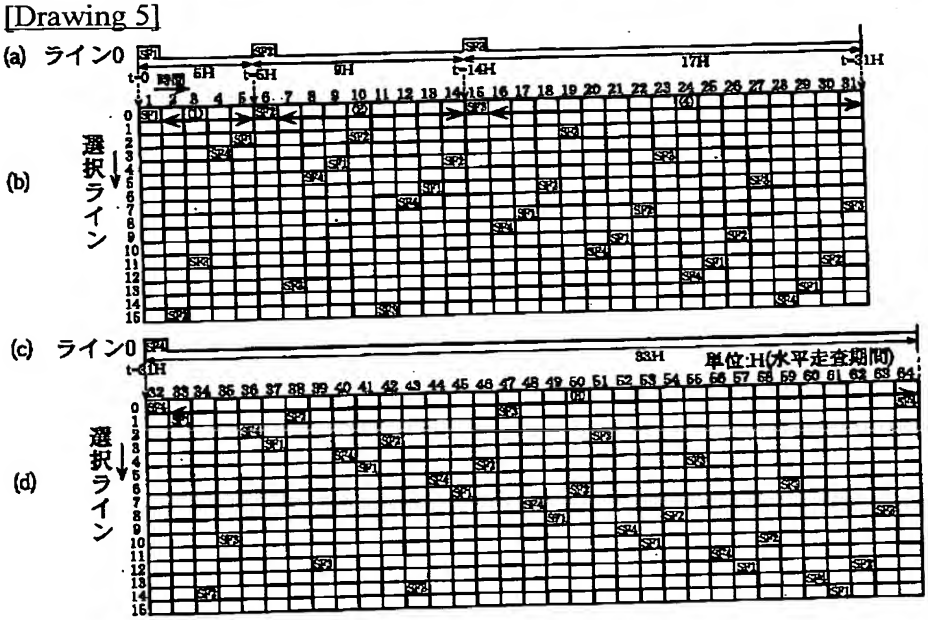
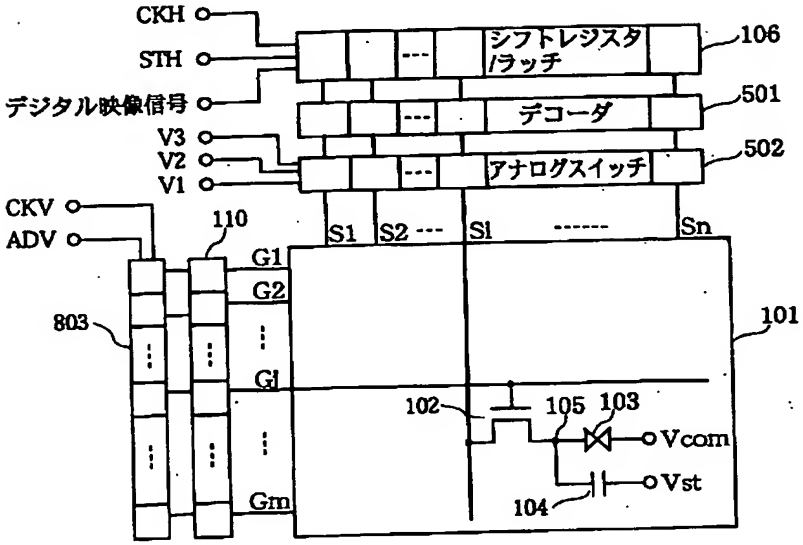
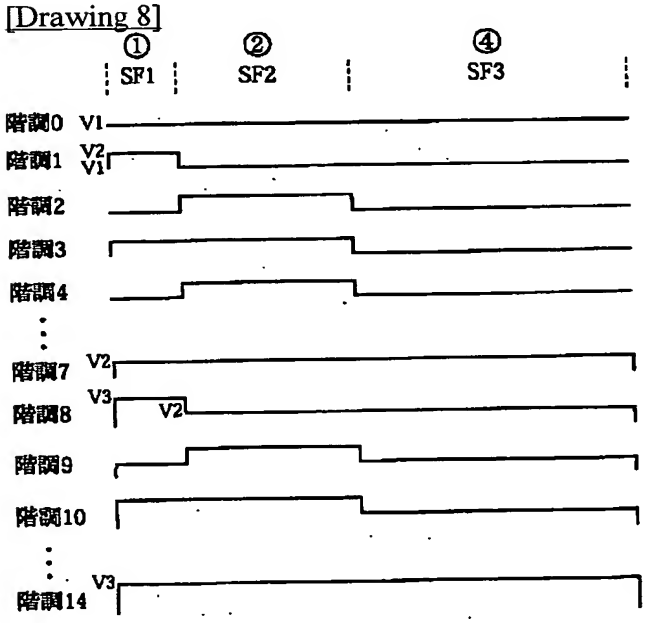


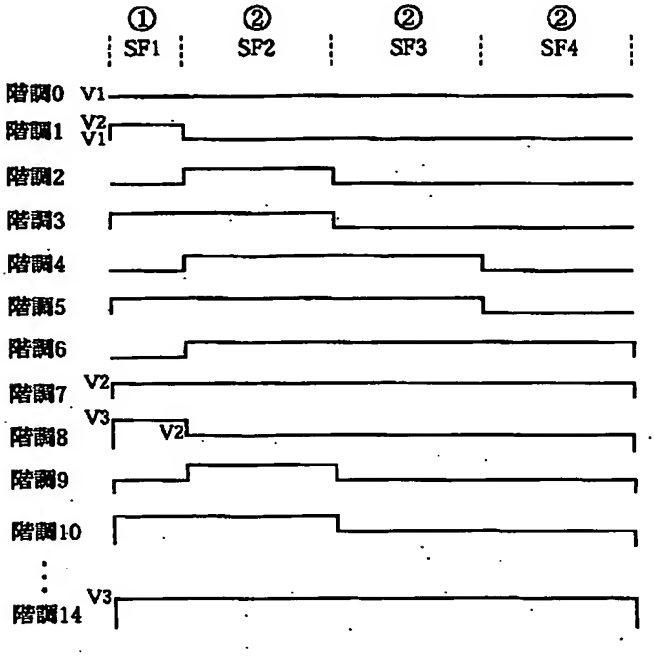
[Drawing 6]



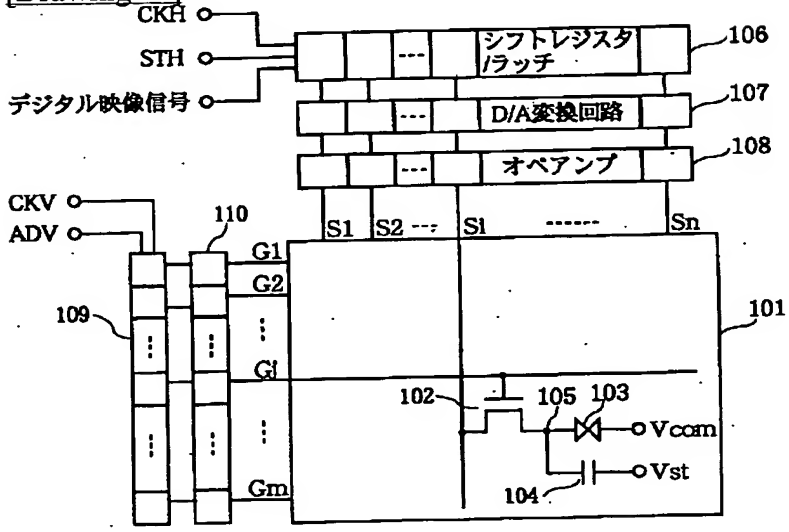
[Drawing 8]



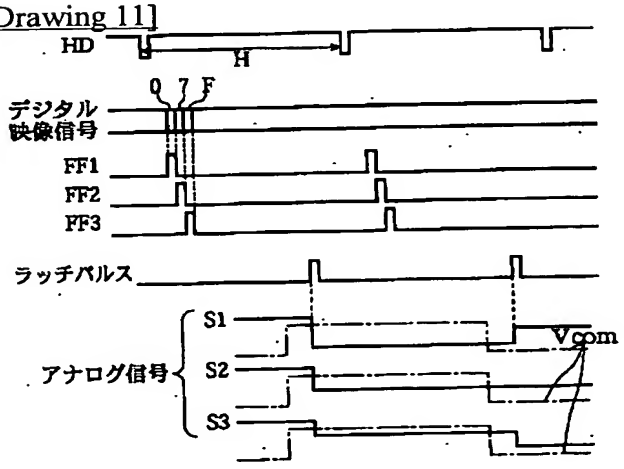
[Drawing 9]



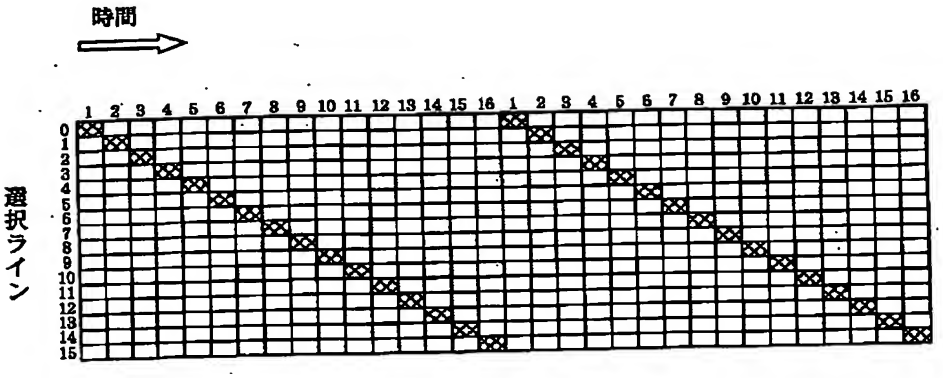
[Drawing 10]



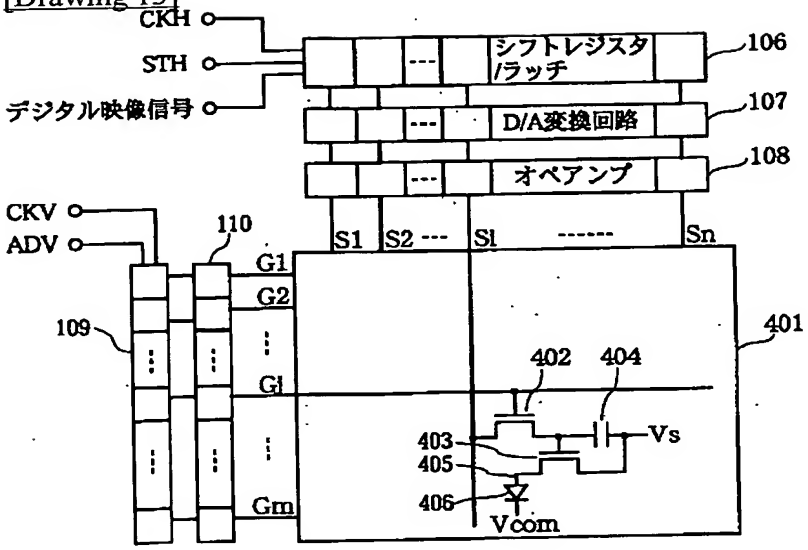
[Drawing 11]



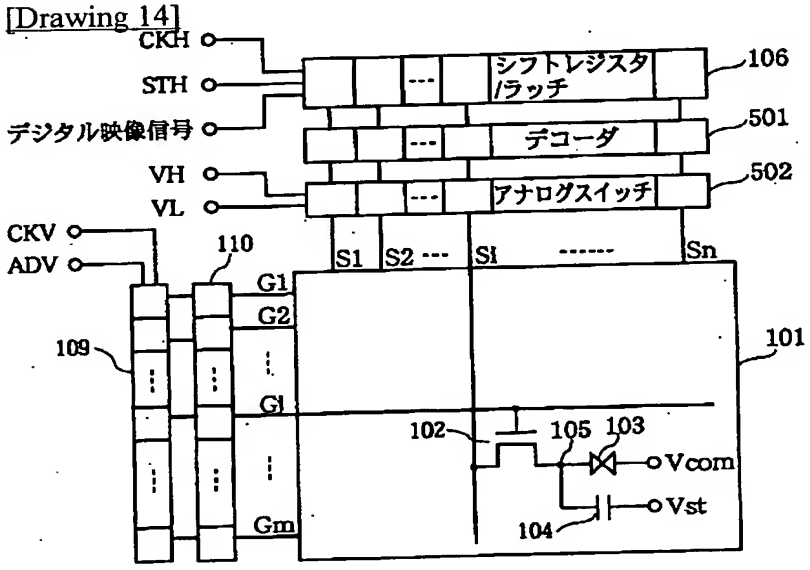
[Drawing 12]



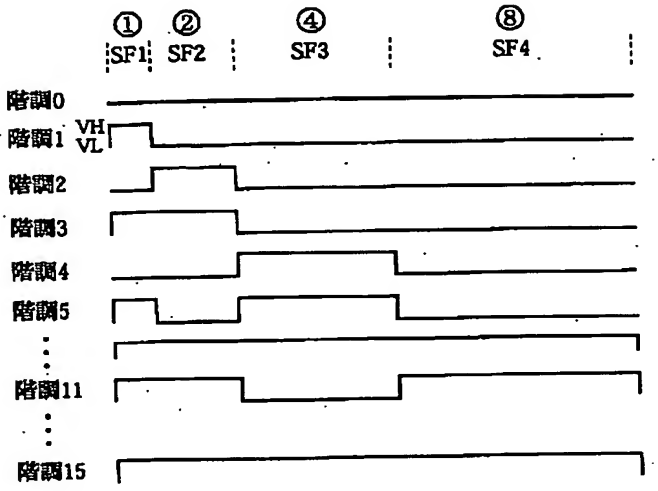
[Drawing 13]



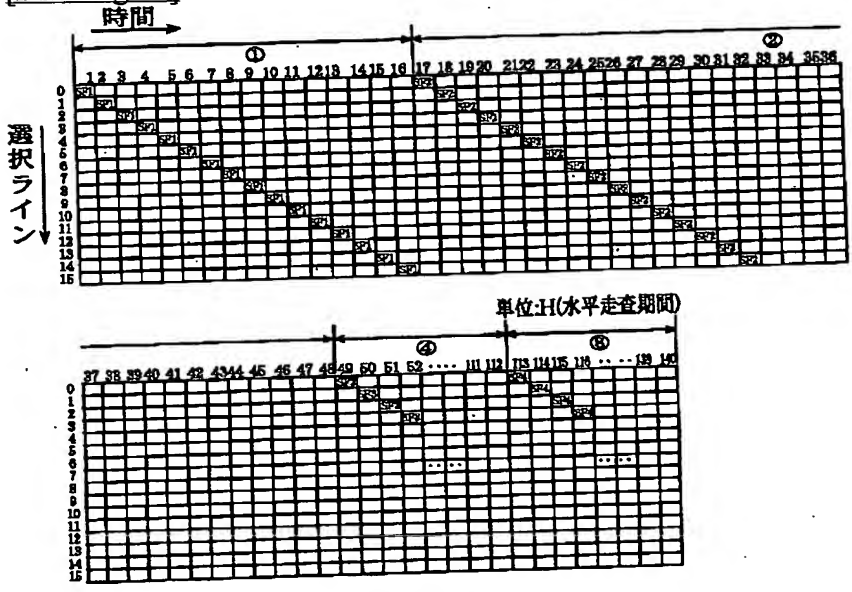
[Drawing 14]



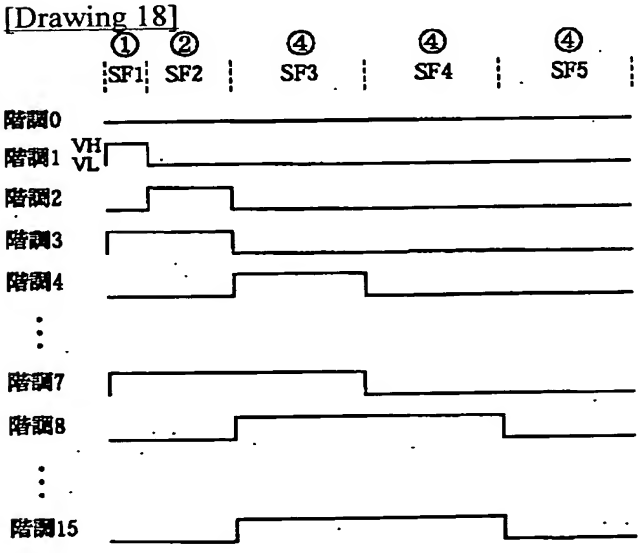
[Drawing 15]



[Drawing 16]



[Drawing 18]



[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] In the drive approach of an active-matrix mold display of constituting from two or more subframes which write in one frame and consist of a period and a maintenance period, and performing a gradation display by the summation effect of said maintenance period While preparing beforehand two or more signal level fewer than the number of display gradation, choosing the value of either of said two or more signal level according to digital image data and outputting through a signal line At the maintenance period for every subframe about the one scanning line defined beforehand the scanning line of the remainders other than said one scanning line defined beforehand If a random scan is carried out according to the sequence it was determined beforehand that did not write in the same subframe about the same scanning line and it sees as the whole one-frame period, it will set to each of each scanning line. The drive approach of the active-matrix mold display characterized by performing the writing for said two or more subframes of every substantially, securing the maintenance period for every subframe and performing a gradation display drive.
[Claim 2] In the drive approach of an active-matrix mold display of constituting from two or more subframes SF1, SF2, --, SFn (n being the natural number) which write in one frame and consist of a period and a maintenance period, and performing a gradation display by the summation effect of said maintenance period While preparing beforehand two or more signal level fewer than the number of display gradation, choosing the value of either of said two or more signal level according to digital image data and outputting through a signal line The selection sequence of said subframe period is SF1->SF2->... ->SFn->SF1->SF2-> ... The drive approach of the active-matrix mold display characterized by choosing the scanning line so that it may circulate with ->SFn.
[Claim 3] In the drive approach of an active-matrix mold display of constituting from two or more subframes SF1, SF2, --, SFn (n being the natural number) which write in one frame and consist of a period and a maintenance period, and performing a gradation display by the summation effect of said maintenance period While preparing beforehand two or more signal level fewer than the number of display gradation, choosing the value of either of said two or more signal level according to digital image data and outputting through a signal line The selection sequence of said subframe period is SF1->SF2->... ->SFn->SF1->SF2-> ... It circulates with ->SFn. And the drive approach of the active-matrix mold display characterized by choosing the scanning line so that it may be scanned sequentially, if it sees about said one subframe period.
[Claim 4] In the drive approach of an active-matrix mold display of constituting from two or more subframes which write in one frame and consist of a period and a maintenance period, and performing a gradation display by the summation effect of said maintenance period While preparing beforehand two or more signal level fewer than the number of display gradation, choosing the value of either of said two or more signal level according to digital image data and outputting through a signal line It is weighting of H and a maintenance period about N and a horizontal scanning period in the number of subframes 1:2:4 : ... When ** (N-1) of :2 and the number of scanning lines are set to L and a positive integer is set to K, The drive approach of the active-matrix mold display by which it is driving [set up said frame period with NH(1+K (Nth power of 2 - 1)) =NHL, and]-it characterized.
[Claim 5] In the drive approach of an active-matrix mold display of constituting from two or more subframes which write in one frame and consist of a period and a maintenance period, and performing a gradation display by the summation effect of said maintenance period While preparing

beforehand two or more signal level fewer than the number of display gradation, choosing the value of either of said two or more signal level according to digital image data and outputting through a signal line when weighting of a maintenance period [in / the number of subframes and / for a horizontal scanning period / H and the i-th subframe period] is set to K (i) (however, i= -- referred to as 1, 2, --, N) and the number of scanning lines is set to L [N] The drive approach of the active-matrix mold display characterized by setting up said frame period with NH(1+sigmaK (i)) =NHL, and driving it.

[Claim 6] In the drive approach of an active-matrix mold display of constituting from two or more subframes which write in one frame and consist of a period and a maintenance period, and performing a gradation display by the summation effect of said maintenance period While preparing beforehand two or more three or more signal level fewer than the number of display gradation, choosing the value of either of said two or more signal level according to digital image data and outputting through a signal line The drive approach of the active-matrix mold display characterized by setting to 2 the degree of freedom of said signal level obtained for said one-frame period to one gradation.

[Claim 7] The drive approach of a active-matrix mold display given in claim 1 thru/or any of 5 they are. [which is characterized by making binary said two or more signal level]

[Claim 8] The drive approach of a active-matrix mold display given in claim 1 thru/or any of 5 they are. [which is characterized by making said two or more signal level into three or more two or more values]

[Claim 9] The 1st substrate with which the storage capacitance connected to the pixel electrode connected to the switching element and said switching element corresponding to each intersection of two or more signal lines arranged in the shape of a matrix and two or more scanning lines and said pixel electrode was formed, It has the 2nd substrate with which the counterelectrode which confronts each other through said the 1st substrate and liquid crystal layer was formed.

(19)日本国特許庁（ＪＰ）　(12)**公開特許公報（Ａ）**　(11)特許出願公開番号
特開2002－175039
（P2002－175039A）
(43)公開日　平成14年６月21日(2002.6.21)

(51)Int.Cl.'	識別記号	ＦＩ	テーマコード（参考）
Ｇ０９Ｇ　3/20	６４１	Ｇ０９Ｇ　3/20	６４１Ｅ　２Ｈ０９３
			６４１Ｃ　５Ｃ００６
			６４１Ｋ　５Ｃ０８０
			６４１Ｒ
	６１１		６１１Ｅ

審査請求　未請求　請求項の数33　ＯＬ　（全 20 頁）　最終頁に続く

(21)出願番号　特願2001－6940(P2001－6940)
(22)出願日　平成13年１月15日(2001.1.15)
(31)優先権主張番号　特願2000－5503(P2000－5503)
(32)優先日　平成12年１月14日(2000.1.14)
(33)優先権主張国　日本（ＪＰ）
(31)優先権主張番号　特願2000－97305(P2000－97305)
(32)優先日　平成12年３月31日(2000.3.31)
(33)優先権主張国　日本（ＪＰ）
(31)優先権主張番号　特願2000－300063(P2000－300063)
(32)優先日　平成12年９月29日(2000.9.29)
(33)優先権主張国　日本（ＪＰ）

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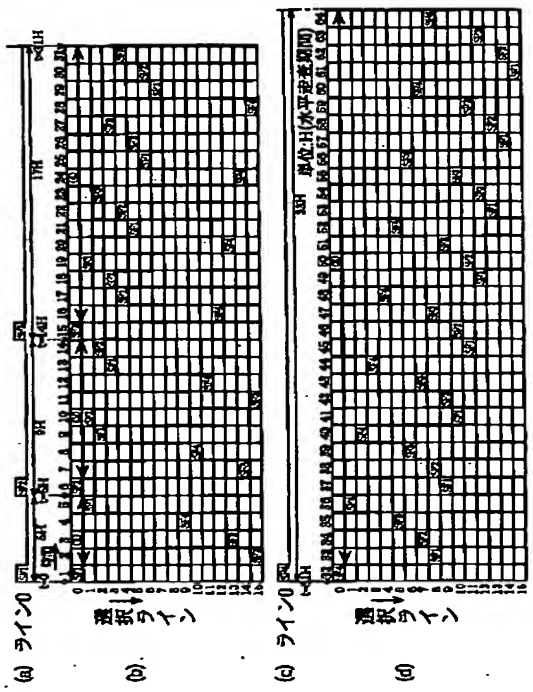
(54)【発明の名称】　アクティブマトリクス型表示装置及びその駆動方法

(57)【要約】
【課題】　サブフレームにより多階調表示を行い、しかもフレーム期間を短縮してフリッカの発生を防止するようにしたアクティブマトリックス型表示装置及びその駆動方法を提供することである。
【解決手段】　１フレームを書き込み期間と保持期間からなる複数のサブフレームで構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置の駆動方法において、予め定めた１つの走査線に関する各サブフレーム毎の保持期間に、前記予め定めた１つの走査線以外の残余の走査線を、同一走査線に関して同一のサブフレームを書き込まないように予め定めた順序に従ってランダム走査し、１フレーム期間全体としてみると、各走査線それぞれにおいて、実質的に前記複数のサブフレーム毎の書き込み及び保持期間が確保されて階調表示駆動が行われる。



【特許請求の範囲】

【請求項１】１フレームを書き込み期間と保持期間からなる複数のサブフレームで構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置の駆動方法において、

表示階調数よりも少ない複数の信号レベルを予め準備しておき、デジタル画像データに応じて、前記複数の信号レベルのうちのいずれかの値を選択して信号線を介して出力するとともに、

予め定めた１つの走査線に関する各サブフレーム毎の保持期間に、前記予め定めた１つの走査線以外の残余の走査線を、同一走査線に関して同一のサブフレームを書き込まないように予め定めた順序に従ってランダム走査し、

１フレーム期間全体としてみると、各走査線それぞれにおいて、実質的に前記複数のサブフレーム毎の書き込みが行われ、各サブフレーム毎の保持期間が確保されて階調表示駆動が行われることを特徴とするアクティブマトリクス型表示装置の駆動方法。

【請求項２】１フレームを書き込み期間と保持期間からなる複数のサブフレームＳＦ１，ＳＦ２，…，ＳＦｎ（ｎは自然数）で構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置の駆動方法において、

表示階調数よりも少ない複数の信号レベルを予め準備しておき、デジタル画像データに応じて、前記複数の信号レベルのうちのいずれかの値を選択して信号線を介して出力するとともに、

前記サブフレーム期間の選択順序がＳＦ１→ＳＦ２→・・・→ＳＦｎ→ＳＦ１→ＳＦ２→・・・→ＳＦｎと循環するように走査線を選択することを特徴とするアクティブマトリクス型表示装置の駆動方法。

【請求項３】１フレームを書き込み期間と保持期間からなる複数のサブフレームＳＦ１，ＳＦ２，…，ＳＦｎ（ｎは自然数）で構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置の駆動方法において、

表示階調数よりも少ない複数の信号レベルを予め準備しておき、デジタル画像データに応じて、前記複数の信号レベルのうちのいずれかの値を選択して信号線を介して出力するとともに、

前記サブフレーム期間の選択順序がＳＦ１→ＳＦ２→・・・→ＳＦｎ→ＳＦ１→ＳＦ２→・・・→ＳＦｎと循環し、かつ１つの前記サブフレーム期間について見れば順次走査となるように走査線を選択することを特徴とするアクティブマトリクス型表示装置の駆動方法。

【請求項４】１フレームを書き込み期間と保持期間からなる複数のサブフレームで構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置の駆動方法において、

表示階調数よりも少ない複数の信号レベルを予め準備しておき、デジタル画像データに応じて、前記複数の信号レベルのうちのいずれかの値を選択して信号線を介して出力するとともに、

サブフレーム数をＮ、水平走査期間をＨ、保持期間の重み付けを１：２：４：・・・：２の（Ｎ－１）乗、走査線数をＬ、正の整数をＫとしたとき、前記フレーム期間をＮＨ（１＋Ｋ（２のＮ乗－１））＝ＮＨＬと設定して駆動すること特徴とするアクティブマトリクス型表示装置の駆動方法。

【請求項５】１フレームを書き込み期間と保持期間からなる複数のサブフレームで構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置の駆動方法において、

表示階調数よりも少ない複数の信号レベルを予め準備しておき、デジタル画像データに応じて、前記複数の信号レベルのうちのいずれかの値を選択して信号線を介して出力するとともに、

サブフレーム数をＮ、水平走査期間をＨ、ｉ番目のサブフレーム期間における保持期間の重み付けをＫ（ｉ）（但し、ｉ＝１，２，…，Ｎとする）、走査線数をＬとしたとき、前記フレーム期間をＮＨ（１＋ΣＫ（ｉ））＝ＮＨＬと設定して駆動することを特徴とするアクティブマトリクス型表示装置の駆動方法。

【請求項６】１フレームを書き込み期間と保持期間からなる複数のサブフレームで構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置の駆動方法において、

表示階調数よりも少なく且つ３以上の複数の信号レベルを予め準備しておき、デジタル画像データに応じて、前記複数の信号レベルのうちのいずれかの値を選択して信号線を介して出力するとともに、１つの階調に対して前記１フレーム期間にとり得る前記信号レベルの自由度を２とすることを特徴とするアクティブマトリックス型表示装置の駆動方法。

【請求項７】前記複数の信号レベルを２値とすることを特徴とする請求項１乃至５の何れかに記載のアクティブマトリクス型表示装置の駆動方法。

【請求項８】前記複数の信号レベルを３以上の複数値とすることを特徴とする請求項１乃至５の何れかに記載のアクティブマトリクス型表示装置の駆動方法。

【請求項９】マトリクス状に配置された複数の信号線と複数の走査線の各交点に対応してスイッチング素子、前記スイッチング素子に接続された画素電極、および前記画素電極に接続された蓄積容量が形成された第１の基板と、前記第１の基板と液晶層を介して対峙する対向電極が形成された第２の基板とを備え、１フレームを書き込み期間と保持期間からなる複数のサブフレームで構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置において、

3

表示階調数よりも少ない複数の電圧レベルを予め準備しておき、デジタル画像データに応じて、前記複数の電圧レベルのうちのいずれかの値を選択して前記信号線を介して出力する信号線駆動回路と、

前記複数の走査線のうち予め定めた１つの走査線に関する各サブフレーム毎の保持期間に、前記予め定めた１つの走査線以外の残余の走査線を、同一走査線に関して同一のサブフレームを書き込まないように予め定めた順序に従ってランダム走査する走査線駆動回路と、を有し、

１フレーム期間全体としてみると、各走査線それぞれにおいて、実質的に前記複数のサブフレーム毎の書き込みが行われ、各サブフレーム毎の保持期間が確保されて階調表示駆動が行われることを特徴とするアクティブマトリックス型表示装置。

【請求項１０】マトリクス状に配置された複数の信号線と複数の走査線の各交点に対応してスイッチング素子、前記スイッチング素子に接続された画素電極、および前記画素電極に接続された蓄積容量が形成された第１の基板と、前記第１の基板と液晶層を介して対峙する対向電極が形成された第２の基板とを備え、１フレームを書き込み期間と保持期間からなる複数のサブフレームＳＦ１，ＳＦ２，…，ＳＦｎ（ｎは自然数）で構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置において、

表示階調数よりも少ない複数の電圧レベルを予め準備しておき、デジタル画像データに応じて、前記複数の電圧レベルのうちのいずれかの値を選択して前記信号線を介して出力する信号線駆動回路と、

前記サブフレーム期間の選択順序がＳＦ１→ＳＦ２→・・・→ＳＦｎ→ＳＦ１→ＳＦ２→・・・→ＳＦｎと循環するように前記走査線を選択する走査線駆動回路と、

を有することを特徴とするアクティブマトリクス型表示装置。

【請求項１１】マトリクス状に配置された複数の信号線と複数の走査線の各交点に対応してスイッチング素子、前記スイッチング素子に接続された画素電極、および前記画素電極に接続された蓄積容量が形成された第１の基板と、前記第１の基板と液晶層を介して対峙する対向電極が形成された第２の基板とを備え、１フレームを書き込み期間と保持期間からなる複数のサブフレームＳＦ１，ＳＦ２，…，ＳＦｎ（ｎは自然数）で構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置において、

表示階調数よりも少ない複数の電圧レベルを予め準備しておき、デジタル画像データに応じて、前記複数の電圧レベルのうちのいずれかの値を選択して前記信号線を介して出力する信号線駆動回路と、

前記サブフレーム期間の選択順序がＳＦ１→ＳＦ２→・・・→ＳＦｎ→ＳＦ１→ＳＦ２→・・・→ＳＦｎと循環し、かつ１つの前記サブフレーム期間について見れば順

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次走査となるように前記走査線を選択する走査線駆動回路と、

を有することを特徴とするアクティブマトリクス型表示装置。

【請求項１２】マトリクス状に配置された複数の信号線と複数の走査線の各交点に対応してスイッチング素子、前記スイッチング素子に接続された画素電極、および前記画素電極に接続された蓄積容量が形成された第１の基板と、前記第１の基板と液晶層を介して対峙する対向電極が形成された第２の基板とを備え、１フレームを書き込み期間と保持期間からなる複数のサブフレームで構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置において、

表示階調数よりも少ない複数の電圧レベルを予め準備しておき、デジタル画像データに応じて、前記複数の電圧レベルのうちのいずれかの値を選択して前記信号線を介して出力する信号線駆動回路と、

サブフレーム数をＮ、水平走査期間をＨ、保持期間の重み付けを１：２：４：・・・：２の（Ｎ－１）乗、走査線数をＬ、正の整数をＫとしたとき、前記フレーム期間をＮＨ（１＋Ｋ（２のＮ乗－１））＝ＮＨＬとなるように、前記走査線を選択する走査線駆動回路と、

を有することを特徴とするアクティブマトリクス型表示装置。

【請求項１３】マトリクス状に配置された複数の信号線と複数の走査線の各交点に対応してスイッチング素子、前記スイッチング素子に接続された画素電極、および前記画素電極に接続された蓄積容量が形成された第１の基板と、前記第１の基板と液晶層を介して対峙する対向電極が形成された第２の基板とを備え、１フレームを書き込み期間と保持期間からなる複数のサブフレームで構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置において、

表示階調数よりも少ない複数の電圧レベルを予め準備しておき、デジタル画像データに応じて、前記複数の電圧レベルのうちのいずれかの値を選択して前記信号線を介して出力する信号線駆動回路と、

サブフレーム数をＮ、水平走査期間をＨ、ｉ番目のサブフレーム期間における保持期間の重み付けをＫ（ｉ）（但し、ｉ＝１，２，…，Ｎとする）、走査線数をＬとしたとき、前記フレーム期間をＮＨ（１＋ΣＫ（ｉ））＝ＮＨＬとなるように、前記走査線を選択する走査線駆動回路と、

を有することを特徴とするアクティブマトリクス型表示装置。

【請求項１４】マトリクス状に配置された複数の信号線と複数の走査線の各交点に対応してスイッチング素子、前記スイッチング素子に接続された画素電極、および前記画素電極に接続された蓄積容量が形成された第１の基板と、前記第１の基板と液晶層を介して対峙する対向電

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極が形成された第２の基板とを備え、１フレームを書き込み期間と保持期間からなる複数のサブフレームで構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置において、
表示階調数よりも少なく且つ３以上の複数の電圧レベルを予め準備しておき、デジタル画像データに応じて、前記複数の電圧レベルのうちのいずれかの値を選択し、しかも１つの階調に対して前記１フレーム期間にとり得る前記電圧レベルの自由度を２とするような選択を行い、この選択された電圧値を前記信号線を介して出力する信号線駆動回路と、
前記走査線を順次走査又はランダム走査する走査線駆動回路と、
を有することを特徴とするアクティブマトリクス型表示装置。
【請求項１５】前記複数の電圧レベルを２値とすることを特徴とする請求項９乃至１３の何れかに記載のアクティブマトリクス型表示装置。
【請求項１６】前記複数の電圧レベルを３以上の複数値とすることを特徴とする請求項９乃至１３の何れかに記載のアクティブマトリクス型表示装置。
【請求項１７】前記信号線駆動回路が複数の前記電圧レベルから１値を選択して出力するアナログマルチプレクサを含むことを特徴とする請求項９乃至１４の何れかに記載のアクティブマトリクス型表示装置。
【請求項１８】前記走査線駆動回路が入力されるアドレス信号に従って走査線を選択するデコーダを含むことを特徴とする請求項９乃至１４の何れかに記載のアクティブマトリクス型表示装置。
【請求項１９】前記スイッチング素子が３端子の薄膜トランジスタで構成されることを特徴とする請求項９乃至１４の何れかに記載のアクティブマトリクス型表示装置。
【請求項２０】前記対向電極を前記信号線駆動回路の出力信号に同期して水平走査期間の整数倍の周期で反転駆動することを特徴とする請求項９乃至１４の何れかに記載のアクティブマトリクス型表示装置。
【請求項２１】前記走査線駆動回路の出力を４値とし、容量結合駆動を行うことを特徴とする請求項９乃至１４の何れかに記載のアクティブマトリクス型表示装置。
【請求項２２】前記走査線駆動回路の出力を２値とし、前記蓄積容量を２値で独立に駆動することにより容量結合駆動を行うことを特徴とする請求項９乃至１４の何れかに記載のアクティブマトリクス型表示装置。
【請求項２３】マトリクス状に配置された複数の信号線と複数の走査線の各交点に対応して第１のスイッチング素子、前記第１のスイッチング素子に接続された第２のスイッチング素子、前記第２のスイッチング素子に接続された画素電極および前記第２のスイッチング素子に前記画素電極と異なる側に接続された電源供給線が形成された第１の基板と、前記第１の基板と発光層を介して対峙する対向電極が形成された第２の基板とを備え、１フレームを書き込み期間と保持期間からなる複数のサブフレームで構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置において、
表示階調数よりも少ない複数の電圧レベルを予め準備しておき、デジタル画像データに応じて、前記複数の電圧レベルのうちのいずれかの値を選択して前記信号線を介して出力する信号線駆動回路と、
前記複数の走査線のうち予め定めた１つの走査線に関する各サブフレーム毎の保持期間に、前記予め定めた１つの走査線以外の残余の走査線を、同一走査線に関して同一のサブフレームを書き込まないように予め定めた順序に従ってランダム走査する走査線駆動回路と、
を有し、
１フレーム期間全体としてみると、各走査線それぞれにおいて、実質的に前記複数のサブフレーム毎の書き込みが行われ、各サブフレーム毎の保持期間が確保されて階調表示駆動が行われることを特徴とするアクティブマトリックス型表示装置。
【請求項２４】マトリクス状に配置された複数の信号線と複数の走査線の各交点に対応して第１のスイッチング素子、前記第１のスイッチング素子に接続された第２のスイッチング素子、前記第２のスイッチング素子に接続された画素電極および前記第２のスイッチング素子に前記画素電極と異なる側に接続された電源供給線が形成された第１の基板と、前記第１の基板と発光層を介して対峙する対向電極が形成された第２の基板とを備え、１フレームを書き込み期間と保持期間からなる複数のサブフレームＳＦ１，ＳＦ２，…，ＳＦｎ（ｎは自然数）で構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置において、
表示階調数よりも少ない複数の電圧レベルを予め準備しておき、デジタル画像データに応じて、前記複数の電圧レベルのうちのいずれかの値を選択して前記信号線を介して出力する信号線駆動回路と、
前記サブフレーム期間の選択順序がＳＦ１→ＳＦ２→・・・→ＳＦｎ→ＳＦ１→ＳＦ２→・・・→ＳＦｎと循環するように前記走査線を選択する走査線駆動回路と、
を有することを特徴とするアクティブマトリクス型表示装置。
【請求項２５】マトリクス状に配置された複数の信号線と複数の走査線の各交点に対応して第１のスイッチング素子、前記第１のスイッチング素子に接続された第２のスイッチング素子、前記第２のスイッチング素子に接続された画素電極および前記第２のスイッチング素子に前記画素電極と異なる側に接続された電源供給線が形成された第１の基板と、前記第１の基板と発光層を介して対峙する対向電極が形成された第２の基板とを備え、１フレームを書き込み期間と保持期間からなる複数のサブフ

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レームＳＦ１，ＳＦ２，…，ＳＦｎ（ｎは自然数）で構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置において、
表示階調数よりも少ない複数の電圧レベルを予め準備しておき、デジタル画像データに応じて、前記複数の電圧レベルのうちのいずれかの値を選択して前記信号線を介して出力する信号線駆動回路と、
前記サブフレーム期間の選択順序がＳＦ１→ＳＦ２→・・・→ＳＦｎ→ＳＦ１→ＳＦ２→・・・→ＳＦｎと循環し、かつ１つの前記サブフレーム期間について見れば順次走査となるように前記走査線を選択する走査線駆動回路と、
を有することを特徴とするアクティブマトリクス型表示装置。

【請求項２６】マトリクス状に配置された複数の信号線と複数の走査線の各交点に対応して第１のスイッチング素子、前記第１のスイッチング素子に接続された第２のスイッチング素子、前記第２のスイッチング素子に接続された画素電極および前記第２のスイッチング素子に前記画素電極と異なる側に接続された電源供給線が形成された第１の基板と、前記第１の基板と発光層を介して対峙する対向電極が形成された第２の基板とを備え、１フレームを書き込み期間と保持期間からなる複数のサブフレームで構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置において、
表示階調数よりも少ない複数の電圧レベルを予め準備しておき、デジタル画像データに応じて、前記複数の電圧レベルのうちのいずれかの値を選択して前記信号線を介して出力する信号線駆動回路と、
サブフレーム数をＮ、水平走査期間をＨ、保持期間の重み付けを１：２：４：・・・：２の（Ｎ－１）乗、走査線数をＬ、正の整数をＫとしたとき、前記フレーム期間をＮＨ（１＋Ｋ（２のＮ乗－１））＝ＮＨＬとなるように、前記走査線を選択する走査線駆動回路と、
を有することを特徴とするアクティブマトリクス型表示装置。

【請求項２７】マトリクス状に配置された複数の信号線と複数の走査線の各交点に対応して第１のスイッチング素子、前記第１のスイッチング素子に接続された第２のスイッチング素子、前記第２のスイッチング素子に接続された画素電極および前記第２のスイッチング素子に前記画素電極と異なる側に接続された電源供給線が形成された第１の基板と、前記第１の基板と発光層を介して対峙する対向電極が形成された第２の基板とを備え、１フレームを書き込み期間と保持期間からなる複数のサブフレームで構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置において、
表示階調数よりも少ない複数の電圧レベルを予め準備しておき、デジタル画像データに応じて、前記複数の電圧レベルのうちのいずれかの値を選択して前記信号線を介して出力する信号線駆動回路と、
サブフレーム数をＮ、水平走査期間をＨ、ｉ番目のサブフレーム期間における保持期間の重み付けをＫ（ｉ）（但し、ｉ＝１，２，…，Ｎとする）、走査線数をＬとしたとき、前記フレーム期間をＮＨ（１＋ΣＫ（ｉ））＝ＮＨＬとなるように、前記走査線を選択する走査線駆動回路と、
を有することを特徴とするアクティブマトリクス型表示装置。

【請求項２８】マトリクス状に配置された複数の信号線と複数の走査線の各交点に対応して第１のスイッチング素子、前記第１のスイッチング素子に接続された第２のスイッチング素子、前記第２のスイッチング素子に接続された画素電極および前記第２のスイッチング素子に前記画素電極と異なる側に接続された電源供給線が形成された第１の基板と、前記第１の基板と発光層を介して対峙する対向電極が形成された第２の基板とを備え、１フレームを書き込み期間と保持期間からなる複数のサブフレームで構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置において、
表示階調数よりも少なく且つ３以上の複数の電圧レベルを予め準備しておき、デジタル画像データに応じて、前記複数の電圧レベルのうちのいずれかの値を選択し、しかも１つの階調に対して前記１フレーム期間にとり得る前記電圧レベルの自由度を２とするような選択を行い、この選択された電圧値を前記信号線を介して出力する信号線駆動回路と、
前記走査線を順次走査又はランダム走査する走査線駆動回路と、
を有することを特徴とするアクティブマトリクス型表示装置。

【請求項２９】前記複数の電圧レベルを２値とすることを特徴とする請求項２３乃至２７の何れかに記載のアクティブマトリクス型表示装置。

【請求項３０】前記複数の電圧レベルを３以上の複数値とすることを特徴とする請求項２３乃至２７の何れかに記載のアクティブマトリクス型表示装置。

【請求項３１】前記信号線駆動回路が複数の前記電圧レベルから１値を選択して出力するアナログマルチプレクサを含むことを特徴とする請求項２３乃至２８の何れかに記載のアクティブマトリクス型表示装置。

【請求項３２】前記走査線駆動回路が入力されるアドレス信号に従って走査線を選択するデコーダを含むことを特徴とする請求項２３乃至２８の何れかに記載のアクティブマトリクス型表示装置。

【請求項３３】前記第１及び第２のスイッチング素子が３端子の薄膜トランジスタで構成されることを特徴とする請求項２３乃至２８の何れかに記載のアクティブマトリクス型表示装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、アクティブマトリクス方式の表示装置、特に液晶、有機ＥＬ（エレクトロルミネッセンス）を用いた表示装置及びその駆動方法に関し、詳しくは時間的に重み付けられたサブフレーム期間における２値あるいは多値の電圧レベルの組み合わせにより多階調表示を行う表示装置及びその駆動方法に関するものである。

【０００２】

【従来の技術】電池駆動による小型の携帯機器に用いられる表示装置には、より少ない消費電力が要求されている。そのような要求を満たす表示デバイスの代表格として、液晶や有機ＥＬ（エレクトロルミネッセンス）が知られている。これらの表示素子を用いたアクティブマトリクス方式の表示装置、典型的には３端子の薄膜トランジスタ（ＴＦＴ）をスイッチング素子とする表示装置では、アナログの電圧あるいは電流によって画素の輝度を制御し階調表示を行うのが一般的である。例えば、液晶の場合はアナログの電圧を印加することによって、有機ＥＬの場合はアナログの電流を流すことによって表示素子の輝度を変化させ階調表示している。

【０００３】従来のアクティブマトリクス液晶パネルの構成を図１０に示し、その階調表示方法を説明する。１０１はアクティブマトリクス方式の液晶パネルであり、信号線Ｓ１～Ｓｎと、これと直交する走査線Ｇ１～Ｇｍと、その交点近傍にあるスイッチング素子からなる。Ｓｉはある信号線、Ｇｊはある走査線、１０２はそれらの交点近傍にあるスイッチング素子、この場合は一般的な３端子の薄膜トランジスタ（ＴＦＴ）の例である。１０３は液晶素子を示し、トランジスタ１０２と対峙する側に対向電極Ｖｃｏｍが形成される。１０４は蓄積容量であり液晶素子１０３の容量成分を補佐し、画質の劣化を防止している。その逆側の電極は別途Ｖｓｔとして共通接続される場合が多い。これらのトランジスタ側の交点１０５が画素電極に相当する。

【０００４】動作を簡単に説明すると、走査線Ｇｊが１フレーム期間に一度高電位となり、トランジスタ１０２を導通させ、この時の信号線Ｓｉの電位まで画素電極１０５、つまり液晶容量１０３と蓄積容量１０４を対向電極Ｖｃｏｍに対して充電する。その後走査線Ｇｊが低電位となってトランジスタ１０２が非導通となって、この充電された電位を１フレーム期間保つ。また、液晶は交流駆動するのが普通であるが、対向電極Ｖｃｏｍと蓄積容量の共通電極Ｖｓｔを信号線Ｓｉに同期して反転したパルス状波形を加え、信号線Ｓｉの振幅を減少することも一般的に行われる。１０６は信号側のシフトレジスタおよびラッチであり、外部から入力されるクロック信号ＣＫＨとスタート信号ＳＴＨにより、映像信号を順次サンプリングしシリアルーパラレル変換する。図１０ではデジタル映像信号の例を示し、複数ビットの映像信号がＤ／Ａ変換回路１０７によりアナログ信号に変えられ、オペアンプ１０８により電流増幅されて信号線Ｓ１～Ｓｎに加えられる。走査側は外部より加えられるクロック信号ＣＫＶとスタート信号ＳＴＶにより順次上から下へ走査するシフトレジスタ１０９と出力バッファ１１０からなり、走査線Ｇ１～Ｇｍをパルス波形で駆動する。

【０００５】図１１に各部の波形図を示す。ＨＤは水平同期信号を示し、その周期は水平走査期間Ｈであり、前述のＳＴＨとＣＫＶの周期に等しい。これらの位相はパネル特性等により若干変えられる。入力信号はデジタル映像信号であり、ＣＫＨの周期でデータは変化する。ＦＦ１，ＦＦ２，ＦＦ３は信号側シフトレジスタのサンプリングパルスを示す。例えば、４ビット、１６階調の場合では、データを１６進数で表現すると、ＦＦ１には”０”、ＦＦ２には”７”、ＦＦ３には”Ｆ”がサンプリングされラッチされている。ラッチパルスのタイミングでこれをＤ／Ａ変換すると、対向電位Ｖｃｏｍに対するパルス高さが変わり、これで階調を表現する。対向反転すれば液晶の交流駆動をする際に信号線の電圧振幅を約１／２にすることが可能で一般的に行われている。なお、図１０の蓄積容量１０４を前段ゲート（図には示されていないがＧｊ－１）とオーバーラップして形成し、前段のゲート側からパルス電圧を印加して、対向電位を一定に保ったまま対向反転同様に信号線の電圧振幅を約１／２に低減できる容量結合駆動がある（特開平３－３５２１８号公報）。あるいは蓄積容量１０４を前段ゲートにオーバーラップさせずに、ゲートとは独立に蓄積容量にパルス電圧を印加する容量結合駆動（特願平１１－２５５２２８）の場合も同様の効果が得られる。

【０００６】図１２に走査線の選択順序を示す。横軸は時間、縦軸は選択ラインである。時間軸の最小幅は水平走査期間Ｈであり、表示ライン数は１６である。図１２のように、選択順序は０→１→２→・・・→１５というように順次走査となっている。従って、１６Ｈで１フレーム期間が完了し、次のフレームの書き込みが始まる。実際には、フレーム期間にはライン選択時間以外に垂直ブランキング期間が設けられるが、図１２では省略している。なお、水平走査期間Ｈは図１１のＨＤの周期に等しく、この時間内にアナログ信号が画素に書き込まれている。次に、従来のアクティブマトリクス有機ＥＬパネルの構成を図１３に示す。図１０の液晶パネルの場合と同機能のものは同一番号を付す。４０１はアクティブマトリクス方式の有機ＥＬパネルであり、信号線Ｓ１～Ｓｎと、これと直交する走査線Ｇ１～Ｇｍと、その交点近傍にあるスイッチング素子からなる。Ｓｉはある信号線、Ｇｊはある走査線、４０２および４０３はそれらの交点近傍にある第１および第２のスイッチング素子であり、３端子の薄膜トランジスタ（ＴＦＴ）を示している。４０４は補助容量であり、第１のトランジスタ４０２を介して第２のトランジスタ４０３のゲート電極に印

加された信号線Ｓｉの電圧を保持する役割をする。４０５の位置は画素電極を示し、第２のトランジスタ４０３を介して電源供給線Ｖｓに接続されている。４０６は有機ＥＬ素子であり、画素電極４０５と対向電極Ｖｃｏｍとの間に形成され、対向電極Ｖｃｏｍおよび電圧供給線Ｖｓとの間に流れる電流により発光し、その電流制御により階調表示を行う。水平駆動回路および垂直駆動回路の動作については図１の液晶の場合と同様であり、走査線Ｇｊを順次走査して第１のトランジスタ４０２を導通させ、信号線Ｓｉに出力されたアナログ電圧を第２のトランジスタ４０３のゲートと補助容量４０４に書き込んでいる。

【０００７】以上のように、従来のアクティブマトリクス液晶パネル及び有機ＥＬパネルでは、アナログ的に輝度を変調することで階調表示を行ってきた。そのため、水平駆動回路にはＤ／Ａ変換回路が設けられ、パネルに対してアナログ量の電圧ないしは電流を出力する必要があった。しかしながら、Ｄ／Ａ変換回路の後段には、負荷である信号線容量を充放電するための電流バッファとしてオペアンプを設ける必要があり、これが駆動回路全体の消費電力を増大させる要因であった。なぜなら、オペアンプは負荷を充放電していないときでもスタティックな電流が絶えず流れて続けており、しかも全信号線数に等しい数だけのオペアンプが存在するので、オペアンプのスタティック電流による消費電力の総和は大きくなり、これが駆動回路全体の消費電力の中で大きな割合を占めていた。

【０００８】またアクティブマトリクス有機ＥＬパネルの階調表示では、有機ＥＬ素子に流れる電流量により輝度を制御するため、パネルの表示品質は画素トランジスタの電流－電圧特性のばらつきに非常に敏感である。したがって、輝度ムラなどの画質低下を防ぐためには、パネル全体にわたりトランジスタ特性を均一に形成する必要がある。

【０００９】これらの電力課題、画質課題を解決する１つの方法として、Ｄ／Ａコンバータやオペアンプなどのアナログ回路を用いず、２値の固定電圧のみを用いて時間変調によりデジタル的に階調表示を行う駆動方法が知られている。本願ではこれをデジタル階調表示方式と呼ぶものとする。デジタル階調表示方式では、アナログ回路のスタティック電流による電力ロスがなく、また高画質に対して要求されるトランジスタ特性のばらつきも厳しくない。

【００１０】図１４に液晶の場合を例として、従来のデジタル階調表示方式の構成を示す。図１４は図１０に比較して、Ｄ／Ａ変換回路およびオペアンプの代わりに、２値の固定電圧ＶＨ、ＶＬを選択するアナログマルチプレクサすなわちデコーダ５０１とアナログスイッチ５０２が配置されている。デコーダとアナログスイッチは非常に簡単な回路で構成することができ、スタティックな電力消費がほとんどない。また、有機ＥＬを用いたデジタル駆動の場合も図５と同様に、Ｄ／Ａ変換回路およびオペアンプの代わりに、デコーダとアナログスイッチが配置される。特に有機ＥＬにデジタル階調表示方式を適用すると、画素トランジスタの電流－電圧特性が多少ばらついても、２値の固定電圧に対する電流変動さえ抑えられれば、輝度ムラが生じない良質な画像を提供できるという利点がある。なお、走査側は図７のように順次走査を行うためのシフトレジスタ回路により構成され、図１０のアナログ駆動と同じである。

【００１１】次に、２値の固定電圧ＶＨ、ＶＬにより階調を表示する方法を図１５と共に説明する。全体画像を表示するフレーム期間を時間的に重み付けされた複数のサブフレーム期間に分け、それぞれのサブフレーム期間において液晶の場合は画素電極に、有機ＥＬの場合は第２のトランジスタのゲート電極にＶＨまたはＶＬを加えることで、時間的なパルス幅変調を行っている。図１５は、固定電圧が２値でサブフレームの数と入力データのビット数が一致している場合の例を示しており、入力データが４ビット、サブフレームの数が４である。入力データの最上位ビット（ＭＳＢ）～最下位ビット（ＬＳＢ）に対応して、サブフレームＳＦ４～ＳＦ１をそれぞれ割り当てている。入力データと重み付けされたサブフレームＳＦ１～ＳＦ４における２値の固定電圧ＶＨ、ＶＬの組み合わせにより１６通りの階調表示を行っている。例えば、階調データが１０進数で１１、すなわち２進数で”１０１１”のとき、サブフレームＳＦ３では”０”に対応するＶＬが選択され、サブフレームＳＦ１、ＳＦ２、ＳＦ４では”１”に対応するＶＨが選択される。なお、液晶素子の透過率－電圧特性（Ｔ－Ｖ特性）や有機ＥＬの発光輝度－電流特性に合わせて、”０”にＶＨ、”１”にＶＬを対応させても良い。

【００１２】従来のデジタル階調表示方式では、時間的に重み付けされたサブフレーム構造をとるために、図１６に示すように走査線を選択する必要がある。図１６はサブフレーム数が４の場合で、単純に走査線を上から下へ順次走査しており、サブフレームの時間的な重み付けを１：２：４：８とするために上位ビットほど長いサブフレーム期間を有している。このように、デジタル駆動で順次走査する場合のフレーム周期は、サブフレーム数をＮ、表示ライン数をＬ、水平走査期間をＨとして

Ｌ（１＋２＋４＋・・・＋２の（Ｎ－１）乗）×Ｈ＝（２のＮ乗－１）ＨＬ

と表される。上式から分かるように、サブフレーム数Ｎが増えるとサブフレーム期間が２のＮ乗の項に起因して急激に大きくなる。特に最上位ビット（ＭＳＢ）に対するサブフレーム期間は、他のラインの書き込みを行わない保持期間が非常に増大してしまう。この原因によりフレーム周期が増大してフリッカと呼ばれるちらつきが生じる。逆にフレーム周波数を一定とすると、水平走査周

波数が大きくなって電力の増大を引き起こすという課題があった。

【００１３】次に、デジタル階調表示方式に特有の画質課題である動画疑似輪郭について説明する。図１７に動画疑似輪郭の発生原理を示す。固定電圧が２値、サブフレーム数が４、サブフレームの保持期間の比が１：２：４：８で１６階調表示する場合において、動画表示を想定し、ある画素の２フレーム間の連続的な輝度変化を考える。図１７では、説明を容易にするため、時間的に最上位ビットに対するサブフレームＳＦ４から順に選択している。第１フレームでは階調”７”すなわち”０１１１”が表示され、第２フレームでは階調”８”すなわち”１０００”が表示されたとする。この場合、２フレーム間では”０１１１１０００”が表示されることになる。人間の目には発光パターンが累積され時間的に平均化されるが、フレーム周波数が６０Ｈｚ程度では”・１１１１・・・”の発光パターンに対して本来”７”あるいは”８”の輝度に見えるはずが、階調”１６”の輝度に一瞬見えてしまう。このように、上位ビットの急激な変化が動画疑似輪郭をもたらす。これを防ぐためには一般的に、サブフレームの数を増やし、急激なビット変化を極力抑える手段が用いられる。例えば、図１８のように、サブフレーム数を５とし、サブフレームの保持期間の比を１：２：４：４：４として適切に１６階調を選ぶようにする。このとき、階調”７”から階調”８”へのビット変化が緩やかになり、この階調変化に関する動画疑似輪郭が低減する。ただし、階調”３”から階調”４”への動画疑似輪郭は残る。サブフレームの数をさらに増やせば、動画疑似輪郭をさらに低減できる。このように、動画疑似輪郭を低減しようとすればサブフレームの数を増やす必要があり、従ってフレーム周期が増大し、フレーム周波数を一定とすれば水平走査周波数が増大し、故に電力増大をもたらすという課題があった。

【００１４】

【発明が解決しようとする課題】上記背景技術の課題を要約すれば以下の通りである。

（１）小型の電池駆動の携帯機器に用いられる表示装置、特にアクティブマトリクス方式の液晶及び有機ＥＬ等の表示装置において、Ｄ／Ａコンバータやオペアンプ等のアナログ回路を用いずに、２値の固定電圧のみで時間的に重み付けられたサブフレームにより多階調表示を行うと、フレーム周期が増大しフリッカを発生したり、電力を増大する要因となっていた。

【００１５】（２）また、動画疑似輪郭を低減するためにサブフレームの数を増やすと、さらに電力の増大を引き起こしていた。

【００１６】本発明の目的は、サブフレームにより多階調表示を行い、しかもフレーム期間を短縮してフリッカの発生を防止するようにしたアクティブマトリックス型表示装置及びその駆動方法を提供することである。

【００１７】また、本発明の他の目的は、サブフレームの数を増やすことなく、動画疑似輪郭を低減するようにしたアクティブマトリックス型表示装置及びその駆動方法を提供することである。

【００１８】

【課題を解決するための手段】上記の目的を達成するため、本発明は、１フレームを書き込み期間と保持期間からなる複数のサブフレームで構成し、前記保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置の駆動方法において、表示階調数よりも少ない複数の信号レベルを予め準備しておき、デジタル画像データに応じて、前記複数の信号レベルのうちのいずれかの値を選択して信号線を介して出力するとともに、予め定めた１つの走査線に関する各サブフレーム毎の保持期間に、前記予め定めた１つの走査線以外の残余の走査線を、同一走査線に関して同一のサブフレームを書き込まないように予め定めた順序に従ってランダム走査し、１フレーム期間全体としてみると、各走査線それぞれにおいて、実質的に前記複数のサブフレーム毎の書き込みが行われ、各サブフレーム毎の保持期間が確保されて階調表示駆動が行われることを特徴とする。

【００１９】本発明による選択方法には、サブフレーム期間の選択順序が循環する場合と循環しない場合の両者が含まれる。また、サブフレームの各々について順次走査の場合とそうでない場合の両者が含まれる。

【００２０】上記構成により、従来のデジタル階調表示方式に比べてフレーム期間を短縮でき、フリッカを大幅に低減できる効果がある。

【００２１】また、フレーム周波数を一定とすれば、水平走査期間が大きくすることができ、この時間に行う液晶パネル容量の充放電による電力を低減できる。

【００２２】更に、Ｄ／Ａ変換回路やオペアンプが不要で駆動回路の構成を簡単にすることができ、消費電力の削減を図ることができる。

【００２３】また、本発明は、サブフレーム期間の選択順序がＳＦ１→ＳＦ２→・・・→ＳＦｎ→ＳＦ１→ＳＦ２→・・・→ＳＦｎと循環するように走査線を選択する駆動方法の場合もある。このような駆動方法にあっては、走査線の選択方法としては、サブフレームの各々について必ずしも順次走査とならないこともある。また、本発明は、サブフレーム期間の選択順序がＳＦ１→ＳＦ２→・・・→ＳＦｎ→ＳＦ１→ＳＦ２→・・・→ＳＦｎと循環し、かつ１つの前記サブフレーム期間について見れば順次走査となるように走査線を選択する駆動方法の場合もある。

【００２４】また、本発明は、サブフレーム数をＮ、水平走査期間をＨ、保持期間の重み付けを１：２：４：・・・：２の（Ｎ－１）乗、走査線数をＬ、正の整数をＫとしたとき、前記フレーム期間をＮＨ（１＋Ｋ（２のＮ乗－１））＝ＮＨＬと設定して駆動する場合もある。

【００２５】また、本発明は、サブフレーム数をN、水平走査期間をH、ｉ番目のサブフレーム期間における保持期間の重み付けをK（ｉ）（但し、ｉ＝１，２，…，Nとする）、走査線数をLとしたとき、前記フレーム期間をNH（１＋ΣK（ｉ））＝NHLと設定して駆動する場合もある。

【００２６】また、本発明は、表示階調数よりも少なく且つ３以上の複数の信号レベルを予め準備しておき、デジタル画像データに応じて、前記複数の信号レベルのうちのいずれかの値を選択して信号線を介して出力するとともに、１つの階調に対して前記１フレーム期間にとり得る前記信号レベルの自由度を２とする場合もある。

【００２７】複数の信号レベルは、２値としてもよく、３以上の複数値としてもよい。特に３以上の複数値（多値化）の場合は、デジタルとアナログの併用により階調表示を行うことを意味する。そして、このように多値化した場合には、サブフレーム数を増やさずに表示階調数を増やせる利点がある。そのため、隣り合う２つの階調での急激なビット変化が小さくなるように適切に階調を選べば、サブフレームを増やさずに動画疑似輪郭による画質劣化を抑えることが可能となる。

【００２８】また、本発明は、上記駆動方法を実現するように構成されたアクティブマトリックス型表示装置である。

【００２９】また、アクティブマトリックス型表示装置としては、液晶層を有する液晶表示装置であってもよく、また、液晶層に代えて、発光層を備えた有機ＥＬ表示装置であってもよい。

【００３０】

【発明の実施の形態】（実施の形態１）図１は実施の形態１に係るアクティブマトリクス型液晶表示装置１０の要部構成図であり、図２は液晶表示装置１０の電気的構成を示す回路図である。本実施の形態１に係る液晶表示装置において、図１０及び図１４に示す従来例に対応する部分には同一の参照符号を付して、詳細な説明は省略する。この液晶表示装置１０は、１フレームを書き込み期間と保持期間からなる複数のサブフレームＳＦ１，ＳＦ２，…，ＳＦｎ（総称するときは参照符号ＳＦで示す）で構成し、保持期間の累積効果で階調表示を行うアクティブマトリックス型表示装置である。液晶表示装置１０は、第１の基板１１と、第１の基板１１に対向して配置される第２の基板１２と、基板１１，１２間に封止される液晶層１０３とを有する。第１の基板１１の内側面には、マトリクス状に配置された複数の信号線Ｓ１，Ｓ２，…，Ｓｎ（信号線を総称するとは、参照符号Ｓで示す）と複数の走査線Ｇ１，Ｇ２，…，Ｇｍ（走査線を総称するときは、参照符号Ｇで示す）の各交点に対応してスイッチング素子としての薄膜トランジスタ１０２（ＴＦＴ）、ＴＦＴ１０２に接続された画素電極１０５および画素電極１０５に接続された蓄積容量１０４が形成されている。また、第２の基板１２の内側面には、対向電極１４が形成されている。

【００３１】２０は信号線駆動回路である。この信号線駆動回路２０は、シフトレジスタ／ラッチ回路１０６（図面の簡略化のため、シフトレジスタとラッチを併せて１つのブロックとして示している）と、デコーダ５０１と、アナログスイッチ５０２とを有する。デコーダ５０１及びアナログスイッチ５０２は、アナログマルチプレクサを構成し、デジタル画像データに応じて２値の固定電圧ＶＨ、ＶＬのいずれかを選択する働きをなす。このような構成により、信号線駆動回路２０は、表示階調数よりも少ない複数（本実施の形態１では固定電圧ＶＨ、ＶＬの２値）の電圧レベルを予め準備しておき、デジタル画像データに応じて、前記複数の電圧レベルのうちのいずれかの値を選択して信号線Ｓを介して出力する機能を果たすことになる。

【００３２】また、３０は走査線駆動回路である。この走査線駆動回路３０は、アドレス信号ＡＤＶにより指定された走査線Ｇを選択するデコーダ８０３と、出力バッファ１１０とから構成されている。デコーダ８０３には制御回路（図示せず）から出力されるアドレス信号ＡＤＶが供給され、アドレス信号ＡＤＶによりアドレス指定された走査線が選択されるように構成されている。なお、アドレスの指定順序は、予め制御回路（図示せず）内のメモリに予め記憶されており、このメモリに基づき後述する所定の順序により走査線がランダム走査されることになる。

【００３３】次いで、液晶表示装置１０の駆動方法について説明する。実施の形態１では、全体画像を表示するフレーム期間を時間的に重み付けされた複数のサブフレーム期間に分け、それぞれのサブフレーム期間において２値の固定電圧ＶＨまたはＶＬを選択出力することで、時間的なパルス幅変調を行っている。階調データとサブフレームにおける２値の固定電圧の組み合わせの関係は、例えば図１５に示されるが、図１５と異なる組み合わせであってもよい。

【００３４】次いで、具体的な駆動シーケンスを図３に示す。この図３は第０番目の走査線～第１５番目の走査線の１６本の走査線で、固定電圧が２値で、サブフレームの数と入力階調データのビット数が共に４で一致している場合の例を示している。図３（ａ）及び図３（ｃ）は第０番目の走査線のサブフレームを示している。また、図３（ｂ）及び図３（ｄ）は走査線の選択順序を示している。なお、図３（ａ）及び図３（ｃ）は全体で１フレーム期間を示しており、図３（ｃ）は図３（ａ）に後続するものであるが、図面のスペース等を考慮して２つに分けて描いたに過ぎない。また、同様に、図３（ｂ）及び図３（ｄ）は全体で１フレーム期間を示しており、図３（ｄ）は図３（ｂ）に後続するものであるが、図面のスペース等を考慮して２つに分けて描いたに

過ぎない。

【００３５】以下、図３を参照しつつ、具体的な駆動方法について説明する。各サブフレームＳＦ１～ＳＦ４の期間は書き込み期間と保持期間からなり、書き込み期間はどのサブフレームにおいても１水平走査期間（１Ｈ）で一定であり、保持期間はサブフレームごとに水平走査期間の２の累乗倍の定数倍に重み付けされている。即ち、サブフレームＳＦ１の保持期間は４Ｈとされ、サブフレームＳＦ２の保持期間は８Ｈとされ、サブフレームＳＦ３の保持期間は１６Ｈとされ、サブフレームＳＦ４の保持期間は３２Ｈとされている。

【００３６】ここで、本発明における駆動方法は、フレーム期間の短縮化を目的とするものである。そして、かかる目的達成のため、予め定めた１つの走査線（図３の場合では、第０番目の走査線に相当する）に関する各サブフレーム毎の保持期間に、前記予め定めた１つの走査線以外の残余の走査線（図３の場合では、第１番目～第１５番目の走査線に相当する）を、同一走査線に関して同一のサブフレームを書き込まないように予め定めた順序に従ってランダム走査し、１フレーム期間全体としてみると、全ての走査線に関してサブフレーム毎の書き込み及び保持期間が確保されて階調表示が行われることを特徴とする。

【００３７】ここで、上記目的を達成するための具体的な走査線の選択順序を設定するに際して、先ず、サブフレーム期間を一般化しておく。Ｈを１水平走査期間、Ｎを全サブフレーム数、Ｋを正の整数とするとき、ｉ番目のサブフレーム期間は、（ただし、ｉ＝１，２，・・・，Ｎ）

（１＋２の（ｉ－１）乗×ＮＫ）×Ｈ

と表される。上式の括弧内の第１項は書き込み期間を表し、第２項は保持期間を表している。保持期間は（２の累乗）×（定数Ｋ）×（サブフレーム数Ｎ）×（水平走査期間Ｈ）で表され、サブフレームごとに（２の累乗）の部分が１，２，４，８・・・と重み付けされる。保持期間にＮＫの項を含んでいるのは、後述するようにフレーム期間の短縮に役立つからである。

【００３８】そして、１フレーム期間は、全サブフレーム期間の和であるので、

（Ｎ＋ＮＫ（１＋２＋４＋・・・＋２の（Ｎ－１）乗））×Ｈ＝ＮＨ（１＋Ｋ（２のＮ乗－１））

と表される。

【００３９】図３（ａ），（ｃ）の波形図においては、パルスの部分が書き込み期間、それ以外の部分が保持期間に相当する。

【００４０】走査線の選択順序は、単純に上から下へ順次走査するのでなく、図３（ｂ），（ｄ）に示すように所定の順序で選択することにより、上位ビットにおけるサブフレーム期間の保持期間を利用して他のラインのサブフレームを書き込み、フレーム期間を短縮している。フレーム期間を短縮する具体的な方法は以下の手順で行う。

【００４１】（１）表示走査線数の設定

１フレーム期間には、全てのサブフレームを書き込むために１ラインに対しＮ回の書き込み期間が必要である。従って、表示走査線数がＬであるとき、１フレーム期間に１水平走査期間の（Ｎ×Ｌ）倍の書き込み期間が必要である。すなわち、書き込み期間はＮＨＬで表される。保持期間を利用して他のラインの書き込みを行うとき、最も効率的なのは、

ＮＨ（１＋Ｋ（２のＮ乗－１））＝ＮＨＬ

が成り立つときである。従って、表示走査線数を

Ｌ＝１＋Ｋ（２のＮ乗－１）

となるように選べばよい。

【００４２】図３（ｂ），（ｄ）の例ではサブフレーム数がＮ＝４であるから、表示走査線数はＬ＝１５Ｋ＋１となる。Ｋは正の整数であり、Ｋ＝１，２，３・・・とすると、Ｌ＝１６，３１，４６・・・となる。図３（ｂ），（ｄ）では、Ｋ＝１として表示走査線数Ｌ＝１６、１フレーム期間がＮＨＬ＝６４Ｈとなっている。

【００４３】（２）走査線の選択順序の設定

次いで、走査線の選択順序に関して詳細に説明する。図３はサブフレーム数がＮ＝４、表示走査線数Ｌ＝１６（Ｋ＝１）の場合であり、各サブフレーム期間は５Ｈ、９Ｈ、１７Ｈ、３３Ｈであり、１フレーム期間はこれらの和であって６４Ｈとなる。先頭の第０番目の走査線に注目すると、時刻ｔ＝０から水平走査期間１Ｈの間に、最下位ビットに対するサブフレームＳＦ１を書き込んでいる。その後、保持期間が４Ｈあって、次に第０番目の走査線のＳＦ２を書き込む時刻はｔ＝５Ｈとなる。このＳＦ１の保持期間の間に、他の走査線のサブフレームを書き込んでいる。即ち、ｔ＝１Ｈで第１５番目の走査線のＳＦ２を、ｔ＝２Ｈで第１３番目の走査線のＳＦ３を、ｔ＝３Ｈで第９番目の走査線のＳＦ４を、ｔ＝４Ｈで第１番目の走査線のＳＦ１を書き込んでいる。換言すれば、書き込むサブフレームの順序がＳＦ１→ＳＦ２→ＳＦ３→ＳＦ４→ＳＦ１・・・というように循環している。また、１つのサブフレーム、例えばＳＦ４に注目すれば、選択順序は開始ラインを９として、９→１０→１１→・・・→１５→０→１→・・・→８というように順次走査となっている。他のサブフレームについても、開始ラインが異なるだけで順次走査と言う点では同様である。各サブフレームの開始ラインは、０ライン目に対する各サブフレームの書き込み時刻が決まれば一義的に決まる。このように、サブフレームの保持期間を利用して他のラインのサブフレームを書き込むように走査線を選択すれば、単純に順次走査してサブフレーム構造をとる場合に比べてフレーム期間をＮ／（２のＮ乗－１）倍に短縮できる。

【００４４】例えば図３と図１６は同じ表示走査線数、

同じサブフレーム数であるが、順次走査の図１６のフレーム周期は２４０Ｈであるのに対し、図３では６４Ｈで済む。フレーム周期を短縮できればフリッカと呼ばれるちらつきを防止することができ、またフレーム周波数を一定とすれば水平走査期間を増大でき、この水平走査期間に行う液晶パネル容量の充放電による電力を低減できる。

【００４５】上記の例では、サブフレームの保持期間の比をＳＦ１：ＳＦ２：ＳＦ３：ＳＦ４＝１：２：４：８としたけれども、本発明はこれに限定されるものではなく、例えばＳＦ１：ＳＦ２：ＳＦ３：ＳＦ４＝２：８：１：４に設定しても、上記と同様な考え方で走査線の選択順序を図４に示すようにすれば、フレーム期間の短縮化を図ることができる。

【００４６】また、上記の例では、サブフレーム期間の選択順序がＳＦ１→ＳＦ２→ＳＦ３→ＳＦ４→ＳＦ１・・・というように循環し、かつ１つのサブフレーム期間について見れば順次走査となるように走査線を選択したいたが、本発明はこれに限定されるものではなく、例えば図５に示すように、サブフレーム期間の選択順序がＳＦ１→ＳＦ２→ＳＦ３→ＳＦ４→ＳＦ１・・・と循環するけれども、１つのサブフレーム期間について見れば順次走査とならないような選択を行うようにしてもよい。図５の場合、例えばＳＦ４に注目すれば、選択順序は開始ラインを３として、３→５→７→９→→１１→１３→１５→２→４→・・・１４→３→５→というように２ラインおきの走査となっている。他のラインについても同様に２ラインおきの走査となっている。このような図５に示す走査線の選択であっても、フレーム期間の短縮化を図ることができる。なお、順次走査を行う方が、走査線を指定するアドレス回路を簡略化できる。

【００４７】また、上記の例では、サブフレーム期間を重み付けの小さい順にＳＦ１→ＳＦ２→ＳＦ３→ＳＦ４→ＳＦ１→・・・というように循環して走査線を選択したが、逆に重み付けの大きい順にＳＦ４→ＳＦ３→ＳＦ２→ＳＦ１→ＳＦ４→・・・と循環してもよい。あるいは、重み付けの大きさに関係なく、例えばＳＦ３→ＳＦ１→ＳＦ４→ＳＦ２→ＳＦ３→・・・というようにサブフレーム順序を自由に設定してもよい。

【００４８】また上記の例ではサブフレームの循環する周期をサブフレーム数Ｎ＝４に一致させて４Ｈ周期としたが、Ｎの倍数の範囲、例えばＮ＝４の場合は８Ｈ周期で循環させても良い。またすべてのラインを複数のラインからなるブロックごとに、あるいは数ラインおきに、あるいは偶数ラインと奇数ラインとに分けるなどして、サブフレームの順序を異ならせてもよい。このような場合、サブフレームの各々について必ずしも順次走査とならないことがある。

【００４９】（走査線の選択方法の要約）上記走査線の選択方法を要約すれば、以下の３通りに大別することができる。

【００５０】（１）複数の走査線のうち予め定めた１つの走査線に関する各サブフレーム毎の保持期間に、前記予め定めた１つの走査線以外の残余の走査線を、同一走査線に関して同一のサブフレームを書き込まないように予め定めた順序に従ってランダム走査して、１フレーム期間全体としてみると、各走査線それぞれにおいて、実質的に前記複数の各サブフレーム毎の書き込み・保持期間が確保されている。

【００５１】この選択方法では、サブフレーム期間の選択順序が循環する場合と循環しない場合の両者が含まれる。また、サブフレームの各々について順次走査の場合とそうでない場合の両者が含まれる。この選択方法によれば、保持時間を有効利用することにより、フレーム期間を短縮できるという効果がある。

【００５２】（２）サブフレーム期間の選択順序がＳＦ１→ＳＦ２→・・・→ＳＦｎ→ＳＦ１→ＳＦ２→・・・→ＳＦｎと循環するように走査線を選択する。

【００５３】この選択方法では、サブフレームの各々について必ずしも順次走査とならないこともある。この選択方法によれば、上記の（１）の選択方法に比べて、保持時間をさらに有効利用でき、フレーム期間を最も短縮できるとともに、走査線を指定するアドレス回路を簡略化できるという効果がある。

【００５４】（３）サブフレーム期間の選択順序がＳＦ１→ＳＦ２→・・・→ＳＦｎ→ＳＦ１→ＳＦ２→・・・→ＳＦｎと循環し、かつ１つの前記サブフレーム期間について見れば順次走査となるように走査線を選択する。この選択方法によれば、上記の（１），（２）の選択方法に比べて、走査線を指定するアドレス回路を、構成の簡単なカウンタ回路で構成できるという効果がある。

【００５５】なお、上記の（１）～（３）の選択方法は、走査線の選択方法の考え方が異なるものであるが、結果的には同一の駆動シーケンスとなる場合はある。

【００５６】また、上記の例では、サブフレームの保持期間を（２の累乗）×（定数Ｋ）×（サブフレーム数Ｎ）×（水平走査期間Ｈ）としたが、（２の累乗）×（定数Ｋ）の部分を任意に設定してもよい。一般化すれば、重みの部分（定数Ｋ）×（２の累乗）をＫ（ｉ）に置き換え、保持期間をＮＨ・Ｋ（ｉ）を表し、ｉ番目のサブフレーム期間を、（ただし、ｉ＝１，２，・・・，Ｎ）

（１＋Ｎ・Ｋ（ｉ））×Ｈ

と表すことができる。また１フレーム期間は、全サブフレーム期間の和であるので、

ＮＨ（１＋Ｋ（１）＋Ｋ（２）＋・・・＋Ｋ（Ｎ））＝ＮＨ（１＋ΣＫ（ｉ））

と表される。フレーム期間を短縮するためにこれをＮＨＬと置けば、表示走査線数は

Ｌ＝１＋Ｋ（１）＋Ｋ（２）＋・・・＋Ｋ（Ｎ）＝１＋

ΣK（i）

となる。そして、この場合においても、上記のサブフレームの保持期間を（2の累乗）×（定数K）×（サブフレーム数N）×（水平走査期間H）する場合と同様な考え方に基づいて、走査線の選択順序を設定すればよい。

【００５７】（実施の形態１の補足説明）①本実施の形態では液晶の交流駆動に関しては従来例と同様に対向反転駆動を仮定しており、固定電圧を２値としたが、対向を一定とする場合には固定電圧を正極性及び負極性でそれぞれ２値ずつ、合計４値とすることで適用可能である。なお、前段ゲートの容量結合駆動、あるいは蓄積容量を独立に制御する容量結合駆動を用いれば、固定電圧を２値のままで対向を一定にすることが可能である。

【００５８】②本実施例ではサブフレーム数Ｎ＝４、定数Ｋ＝１より表示ライン数をＬ＝１６としたが、これは表示可能な最大ライン数であって、実際にはこれより少ないライン数でもよい。例えば、表示可能な最大ライン数をＬ＝１６とし、実際に表示するライン数を１５ラインとした場合には、どのラインも選択されない時間が４Ｈ分生じるだけである。

【００５９】（実施の形態２）図６は実施の形態２に係る液晶表示装置１０Ａの電気的構成を示す回路図である。本実施の形態２は、実施の形態１に類似し対応する部分には同一の参照符号を付す。上記実施の形態１では時間的に重み付けされた複数のサブフレームにおける２値の固定電圧の組み合わせで階調表示を行うようにしたが、本実施の形態２では、３値以上の固定電圧を組み合わで階調表示を行うことを特徴するものである。このことは、多値サブフレームによる階調表示、すなわちデジタルとアナログの併用により階調表示を行うことを意味する。

【００６０】このように多値化した場合には、信号側駆動回路の固定電圧を選択するアナログマルチプレクサ（デコーダおよびスイッチ）の回路構成が複雑になるが、サブフレーム数を増やさずに表示階調数を増やせる利点がある。例えば、図７のように、３値４サブフレームで保持期間の比を１：２：４：８とした場合、１つの階調に対して取り得る固定電圧の自由度を２とすれば、最大３１階調得られる。

【００６１】一方、多値化によりサブフレーム数を少なくすることも可能である。例えば、図８のように、３値３サブフレームで保持期間の比を１：２：４とした場合、１つの階調に対して取り得る固定電圧の自由度を２とすれば、最大１５階調得られる。サブフレーム数を少なくできればフレーム周期をさらに短縮することができ、フレーム周波数を一定とすれば水平走査周波数を低減でき、電力を低減することが可能である。ここで多値化する際、１つの階調に対して取り得る固定電圧の自由度を２とすることにより、隣り合う階調間での輝度飛びを防ぐことができ、階調－輝度特性において連続性を保つことができる。

【００６２】また、図９のように、３値４サブフレームで保持期間の比を１：２：２：２として、隣り合う２つの階調での急激なビット変化が小さくなるように適切に階調を選べば、サブフレームを増やさずに動画疑似輪郭による画質劣化を抑えることが可能である。

【００６３】なお、多値化した場合も２値の場合と同様に、対向反転駆動及び容量結合駆動を用いて、固定電圧の数を２倍にすることなく液晶の交流駆動が可能である。

【００６４】（その他の事項）上記実施の形態１，２では表示素子に液晶を用いて説明したが、表示素子が有機ＥＬであっても実施の形態１，２の走査線の選択方法を同様に適用することができる。

【００６５】

【発明の効果】以上のように本発明によれば以下の効果を奏する。

（１）従来のアクティブマトリクス型表示装置、特に液晶、有機ＥＬを用いたアクティブマトリクス型表示装置において、従来のデジタル階調表示方式に比べてフレーム期間を短縮でき、フリッカを大幅に低減できる効果がある。また、フレーム周波数を一定とすれば、水平走査期間が大きくすることができ、この時間に行う液晶パネル容量の充放電による電力を低減できる効果がある。

【００６６】（２）Ｄ／Ａ変換回路やオペアンプが不要でドライバ回路の構成を簡単にすることができ、これらで消費する電力を削減できる効果がある。

【００６７】（３）従来のアナログ階調表示方式で要求されるほど高精度で均一な薄膜トランジスタの特性を必要とせず、トランジスタ特性ばらつきによる輝度ムラなどの画質劣化を低減できる効果がある。

【００６８】（４）固定電圧を多値化することにより、電力を増大させずに階調性や動画疑似輪郭などの画質劣化を防ぐことが可能となる。

【図面の簡単な説明】

【図１】実施の形態１に係るアクティブマトリクス型液晶表示装置１０の要部構成図である。

【図２】液晶表示装置１０の電気的構成を示す回路図である。

【図３】実施の形態１における走査線の選択順序を示す駆動シーケンス図である。

【図４】実施の形態１における走査線の選択順序の変形例を示す駆動シーケンス図である。

【図５】実施の形態１における走査線の選択順序の変形例を示す駆動シーケンス図である。

【図６】実施の形態２に係る液晶表示装置１０Ａの電気的構成を示す回路図である。

【図７】実施の形態２における階調とサブフレームとの関係を示す図である。

【図８】実施の形態２における階調とサブフレームとの

関係の変形例を示す図である。

【図９】実施の形態２における階調とサブフレームとの関係の変形例を示す図である。

【図１０】従来のアクティブマトリクス液晶パネルにおけるアナログ階調表示の構成図である。

【図１１】従来のアクティブマトリクス液晶パネルにおけるアナログ階調表示の波形図である。

【図１２】従来のアナログ階調表示の走査線選択順序を示す図である。

【図１３】従来のアクティブマトリクス有機ＥＬパネルにおけるアナログ階調表示の構成図である。

【図１４】従来のアクティブマトリクス液晶パネルにおけるデジタル階調表示の構成図である。

【図１５】デジタル階調表示における階調とサブフレームの関係を示す図である。

【図１６】従来のデジタル階調表示の走査線選択順序を示す図である。

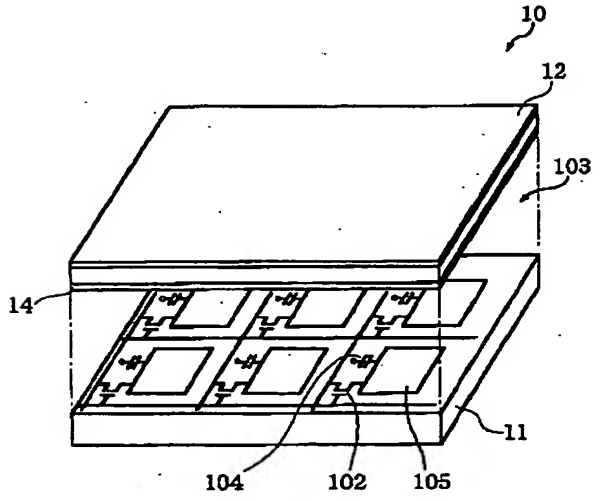
【図１７】デジタル階調表示における動画疑似輪郭の発生原理を示す図である。

【図１８】従来のデジタル階調表示における動画疑似輪郭の低減方法を示す図である。

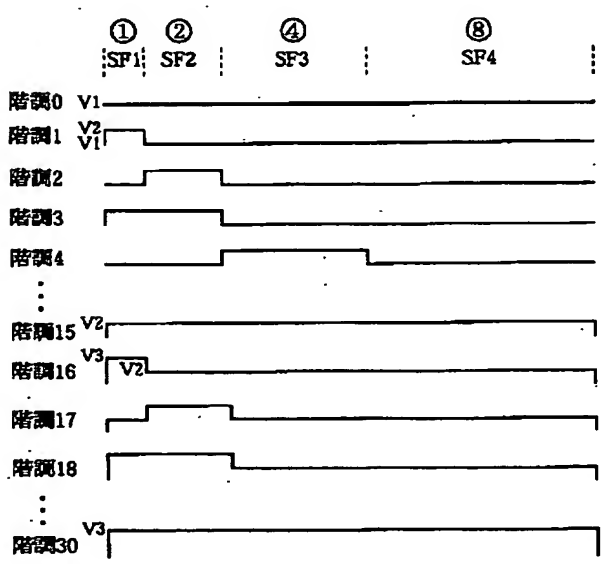
【符号の説明】

１０　：液晶表示装置
２０　：信号側駆動回路
３０　：走査線駆動回路
１０１：液晶パネル
１０２，４０２，４０３：スイッチング素子
１０３：液晶層
１０４：蓄積容量
１０５，４０５：画素電極
１０６：シフトレジスタ及びラッチ
１１０：出力バッファ
４０１：アクティブマトリクス方式の有機ＥＬパネル
４０４：補助容量
４０６：有機ＥＬ素子
５０１：デコーダ
５０２：アナログスイッチ
８０３：走査線選択デコーダ
Ｓ１，Ｓ２，Ｓ３，Ｓｉ，Ｓｎ：信号線
Ｇ１，Ｇ２，Ｇ３，Ｇｊ，Ｇｍ：走査線
ＣＫＨ：信号側クロック信号
ＳＴＨ：信号側スタート信号
ＣＫＶ：走査側クロック信号
ＳＴＶ：走査側クロック信号
ＡＤＶ：走査側アドレス信号
Ｖｃｏｍ：対向電極
Ｖｓｔ：蓄積容量の共通電極
Ｖｓ：電源供給線
ＨＤ：水平同期信号
ＦＦ１，ＦＦ２，ＦＦ３：信号側シフトレジスタのサンプリングパルス
ＶＨ，ＶＬ，Ｖ１，Ｖ２，Ｖ３：固定電圧
ＳＦ１，ＳＦ２，ＳＦ３，ＳＦ４：サブフレーム期間

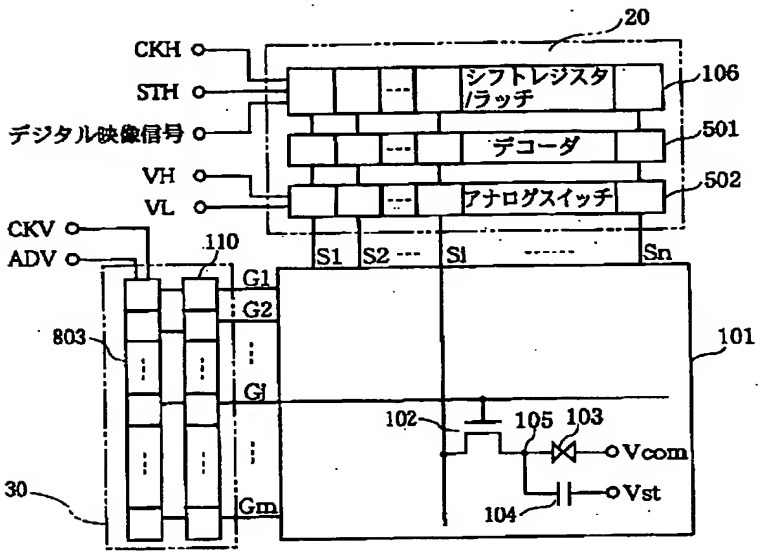
【図１】



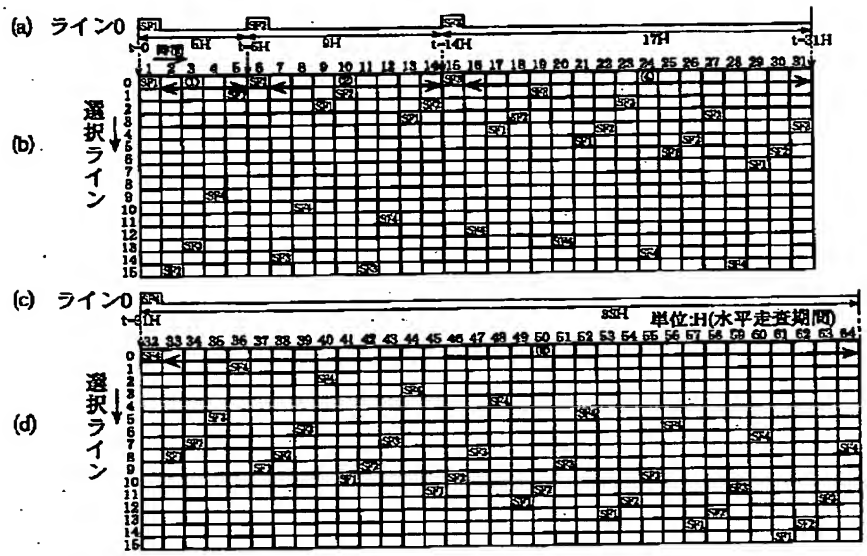
【図７】



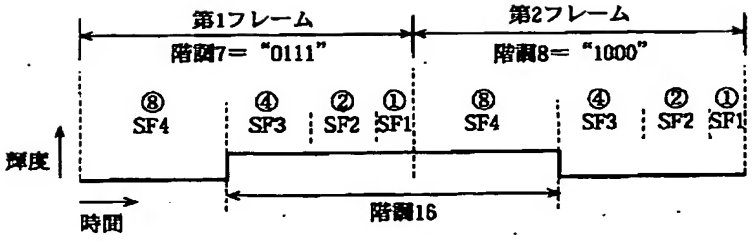
【図２】


20
CKH
STH
デジタル映像信号
VH
VL
CKV
ADV
シフトレジスタ/ラッチ
106
デコーダ
501
アナログスイッチ
502
110
S1
S2
Si
Sn
G1
G2
Gi
Gm
803
101
102
105
103
Vcom
Vst
104
30

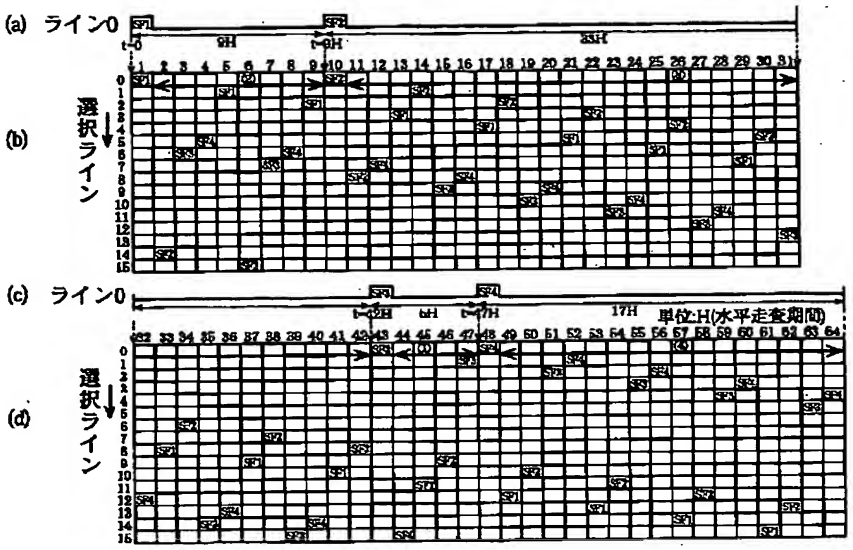
【図３】


(a) ライン0
(b)
選択ライン
(c) ライン0
(d)
選択ライン
単位:H(水平走査期間)

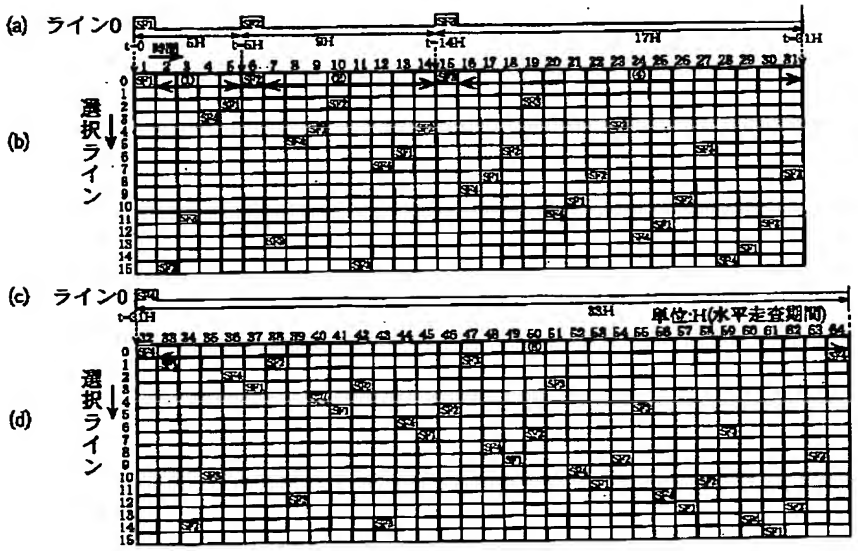
【図１７】


第1フレーム
階調7＝"0111"
第2フレーム
階調8＝"1000"
⑧ SF4
④ SF3
② SF2
① SF1
輝度
時間
階調16

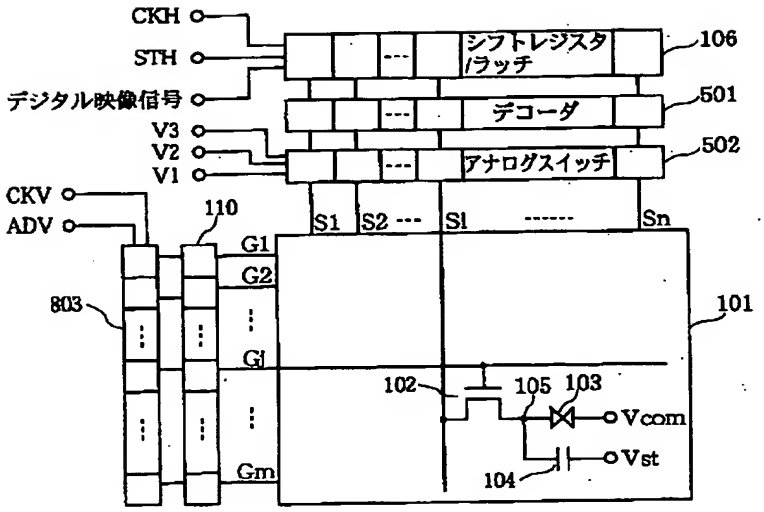
【図４】


(a) ラインO
(b)
選択ライン
(c) ラインO
(d)
選択ライン
単位:H(水平走査期間)

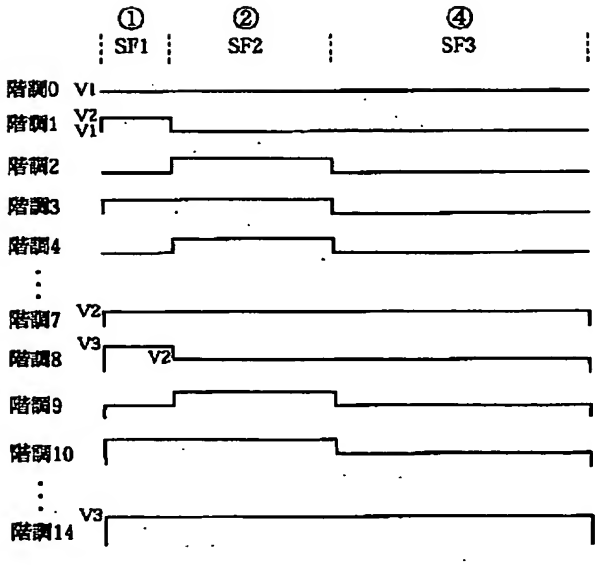
【図５】


(a) ラインO
(b)
選択ライン
(c) ラインO
(d)
選択ライン
単位:H(水平走査期間)

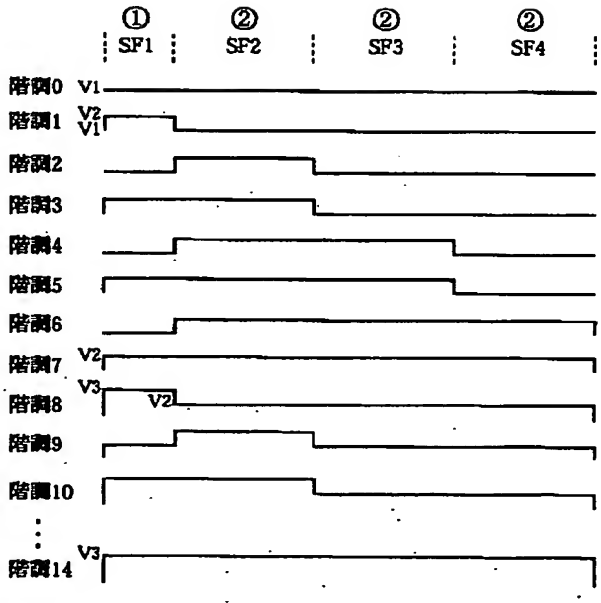
【図６】


CKH
STH
デジタル映像信号
V3
V2
V1
CKV
ADV
シフトレジスタ/ラッチ
デコーダ
アナログスイッチ
106
501
502
110
S1
S2
Si
Sn
G1
G2
Gj
Gm
803
101
102
105
103
Vcom
Vst
104

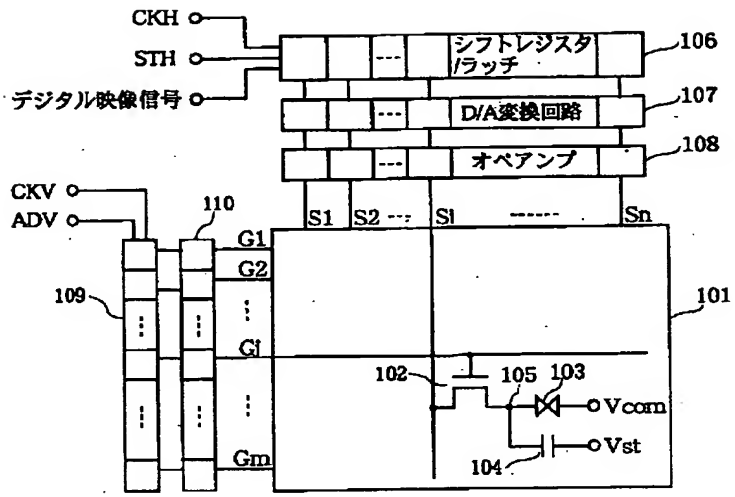
【図８】


①
SF1
②
SF2
④
SF3
階調0
階調1
階調2
階調3
階調4
階調7
階調8
階調9
階調10
階調14
V1
V2
V3

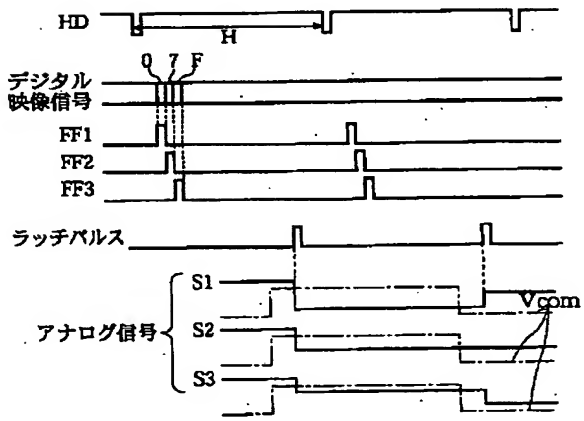
【図９】


①
SF1
②
SF2
②
SF3
②
SF4
階調0
階調1
階調2
階調3
階調4
階調5
階調6
階調7
階調8
階調9
階調10
階調14
V1
V2
V3

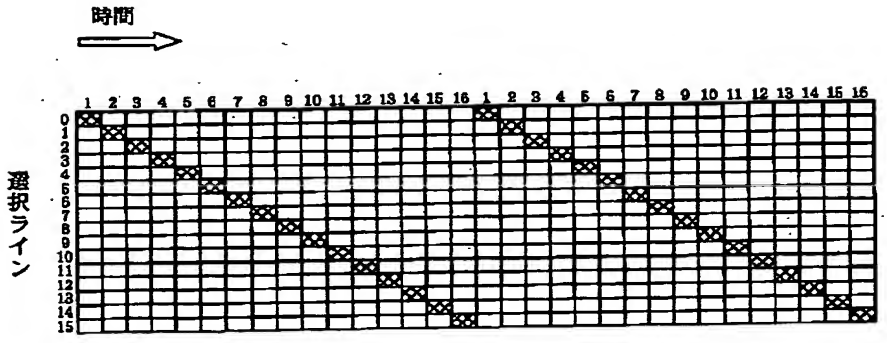
【図１０】


CKH
STH
デジタル映像信号
シフトレジスタ/ラッチ
106
D/A変換回路
107
オペアンプ
108
CKV
ADV
110
S1
S2
Si
Sn
G1
G2
Gi
Gm
109
101
102
105
103
Vcom
Vst
104

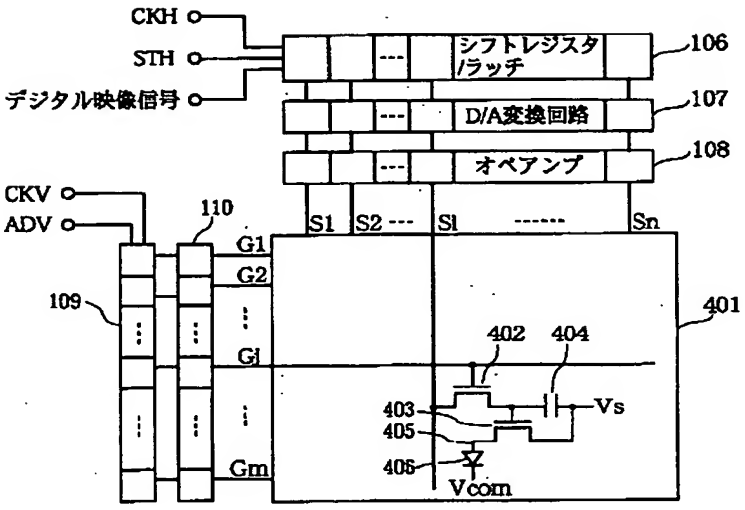
【図１１】


HD
H
0
7
F
デジタル映像信号
FF1
FF2
FF3
ラッチパルス
S1
S2
S3
アナログ信号
Vcom

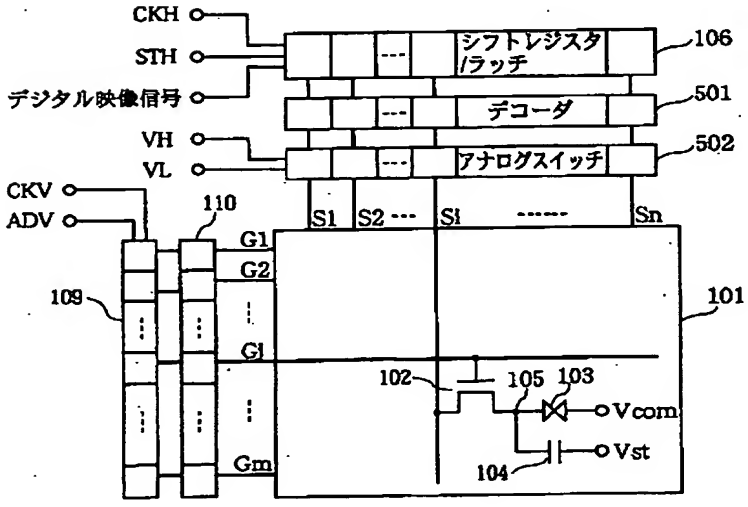
【図１２】


時間
選択ライン
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

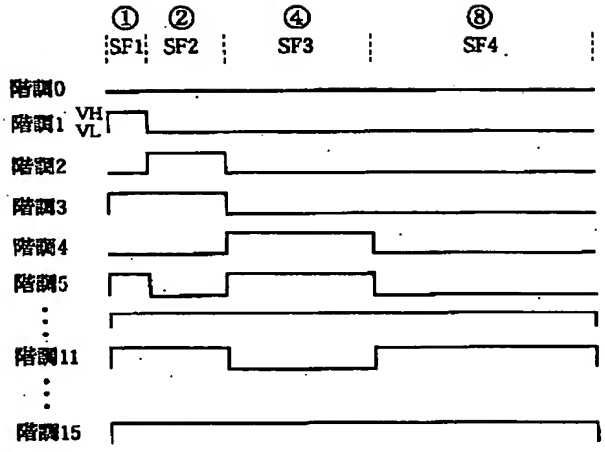
【図１３】


CKH
STH
デジタル映像信号
シフトレジスタ/ラッチ
106
D/A変換回路
107
オペアンプ
108
CKV
ADV
110
S1
S2
Si
Sn
G1
G2
Gi
Gm
109
401
402
404
403
405
406
Vs
Vcom

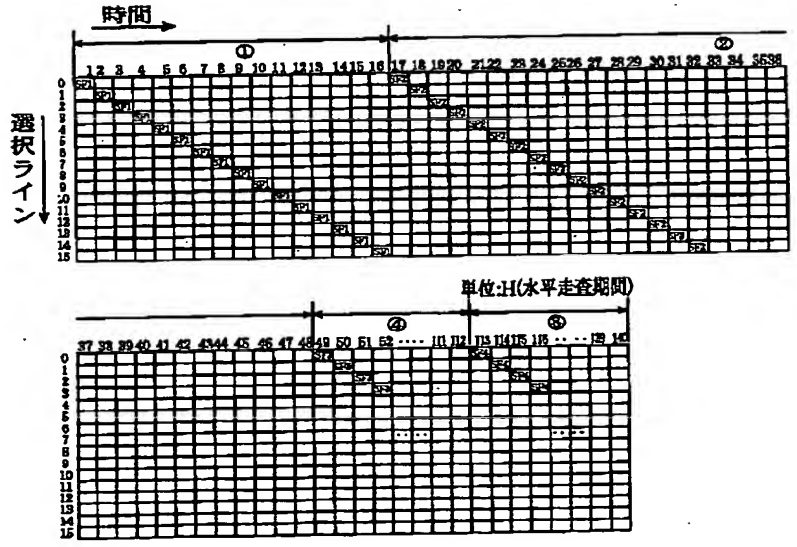
【図１４】


CKH
STH
デジタル映像信号
シフトレジスタ/ラッチ
106
デコーダ
501
VH
VL
アナログスイッチ
502
CKV
ADV
110
S1
S2
Si
Sn
G1
G2
Gi
Gm
109
101
102
105
103
Vcom
Vst
104

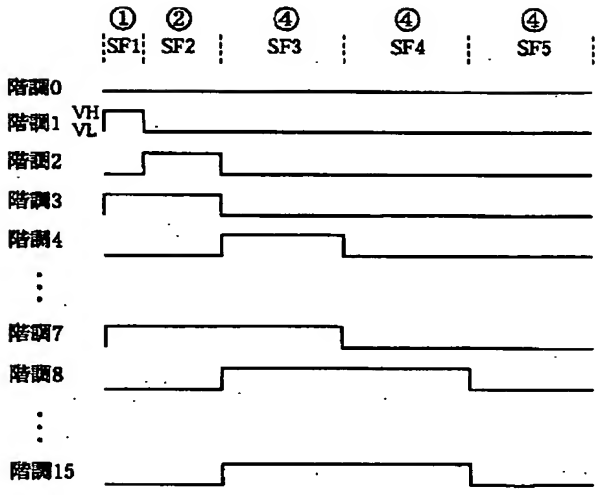
【図１５】


①
②
④
⑧
SF1
SF2
SF3
SF4
階調0
階調1
VH
VL
階調2
階調3
階調4
階調5
階調11
階調15

【図１６】


時間
①
②
選択ライン
単位:H(水平走査期間)
④
⑤

【図１８】



フロントページの続き

(51)Int.Cl.[7]		識別記号	FI		テーマコード(参考)
G09G	3/20	622	G09G	3/20	622E
					622Q
		623			623E
G02F	1/133	550	G02F	1/133	550
G09G	3/30		G09G	3/30	K
	3/36			3/36	

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Fターム(参考)　2H093 NA16 NA51 NC22 NC23 NC26
NC34 ND06 ND10
5C006 AA01 AA14 AA16 AA17 AC28
AF83 BB16 BC03 BC12 BF03
BF04 BF24 BF25 BF26 FA23
FA29 FA56
5C080 AA06 AA10 BB05 DD05 DD06
EE19 EE29 FF11 JJ02 JJ04

整理番号　J0095721
発送番号　120132
発送日　　平成 18 年 3 月 28 日

拒絶理由通知書

特許出願の番号	特願２００３－０２０４３２
起案日	平成１８年　３月２０日
特許庁審査官	濱本　禎広　　９５０９　２Ｇ００
特許出願人代理人	上柳　雅誉（外　２名）　様
適用条文	第２９条第１項、第２９条第２項

＜＜＜＜　　最　　後　　＞＞＞＞

この出願は、次の理由によって拒絶をすべきものである。これについて意見があれば、この通知書の発送の日から６０日以内に意見書を提出して下さい。

理　由

１．この出願の下記の請求項に係る発明は、その出願前に日本国内又は外国において、頒布された下記の刊行物に記載された発明又は電気通信回線を通じて公衆に利用可能となった発明であるから、特許法第２９条第１項第３号に該当し、特許を受けることができない。

２．この出願の下記の請求項に係る発明は、その出願前日本国内又は外国において頒布された下記の刊行物に記載された発明又は電気通信回線を通じて公衆に利用可能となった発明に基いて、その出願前にその発明の属する技術の分野における通常の知識を有する者が容易に発明をすることができたものであるから、特許

法第２９条第２項の規定により特許を受けることができない。

記　　（引用文献等については引用文献等一覧参照）

・請求項　　１－１３
・理由　　１－２
・引用文献等　１
・備考
　引用文献１の段落【００２６】－【００２９】を参照されたい。特に、段落【００２７】には「隣り合う２つの階調での急激なビット変化が小さくなるように適切に階調を選べば」と記載されている。そして、同引用文献の【図７】－【図９】では、隣接サブフレームに供給される電圧レベルは同じものか隣り合うものとなっている。

　この拒絶理由通知書の内容に問い合わせがある場合、または、この案件について面接を希望する場合は、特許審査第一部ナノ物理　濱本 禎広、TEL　03-3581-1101 内 3226、FAX　03-3592-8858　までご連絡ください。

引　用　文　献　等　一　覧

１．特開２００２－１７５０３９号公報

最後の拒絶理由通知とする理由

１．最初の拒絶理由通知に対する応答時の補正によって通知することが必要になった拒絶の理由のみを通知する拒絶理由通知である。